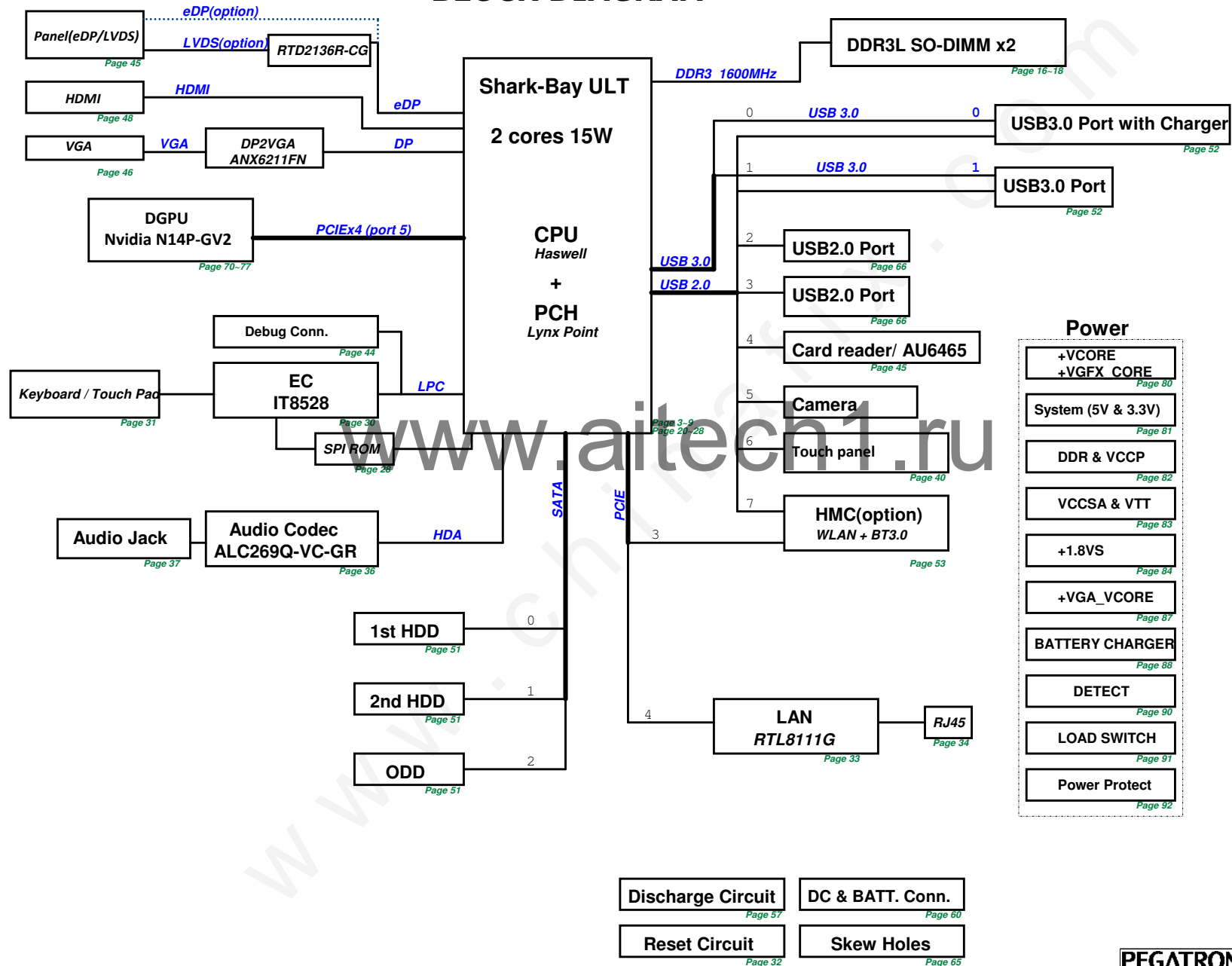
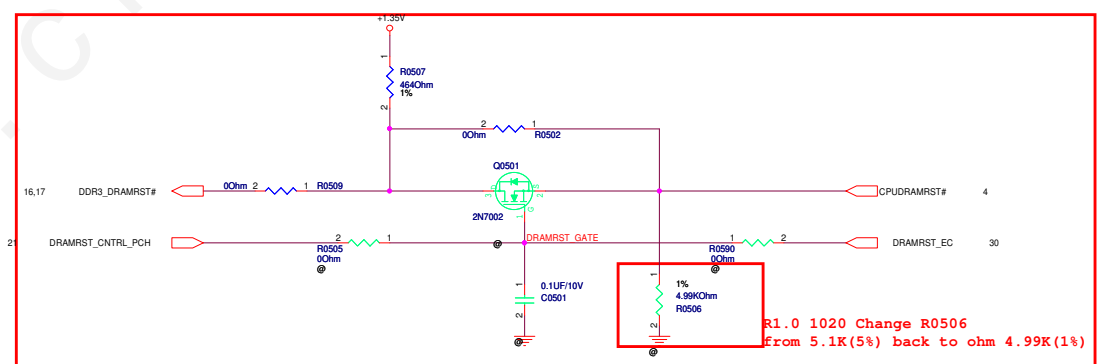
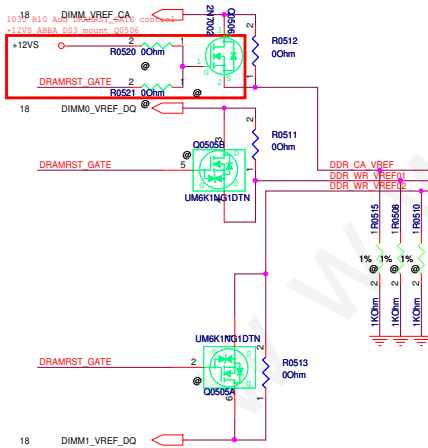
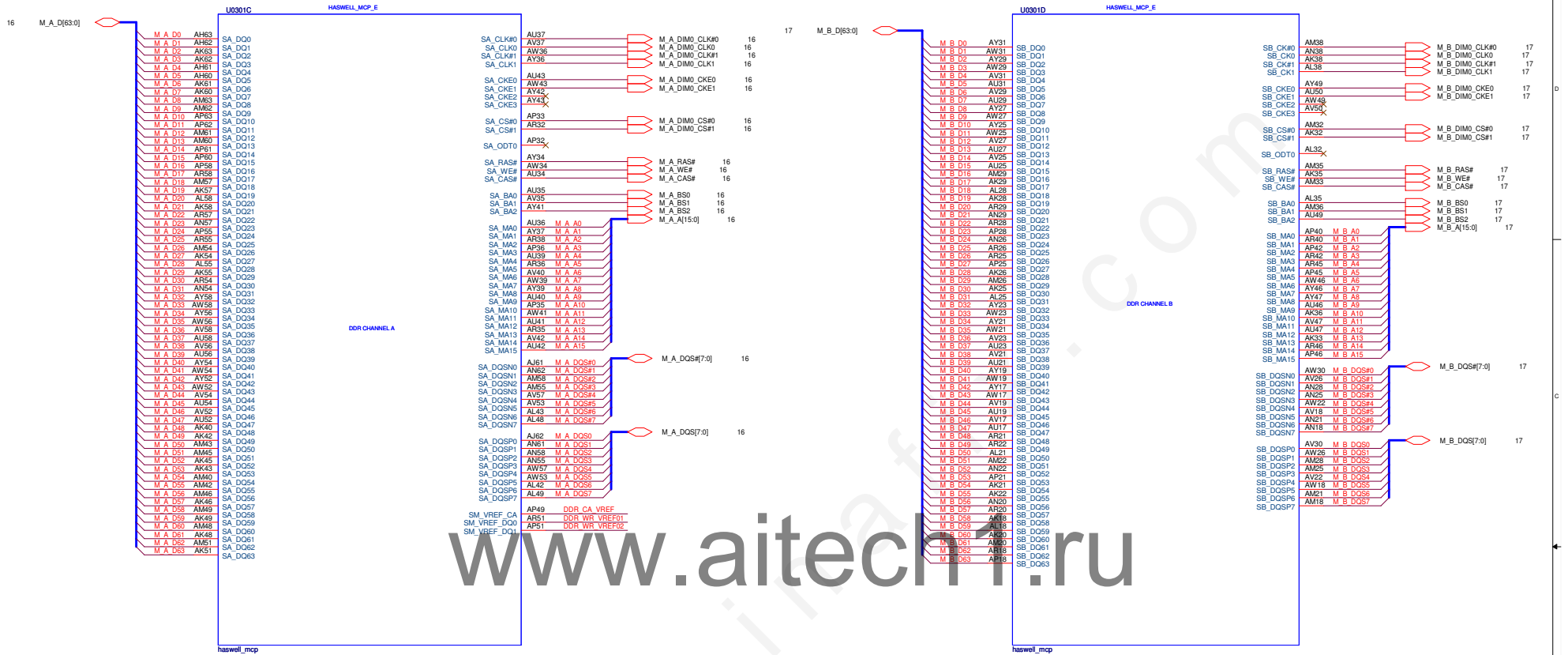
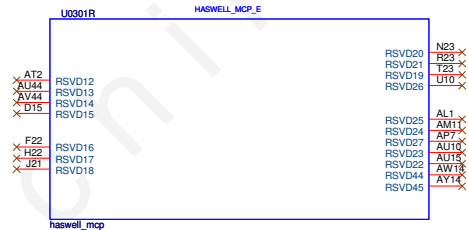
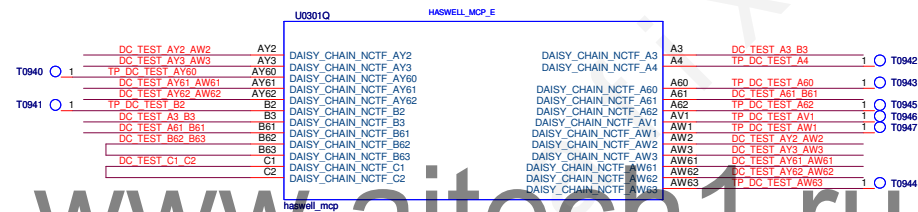
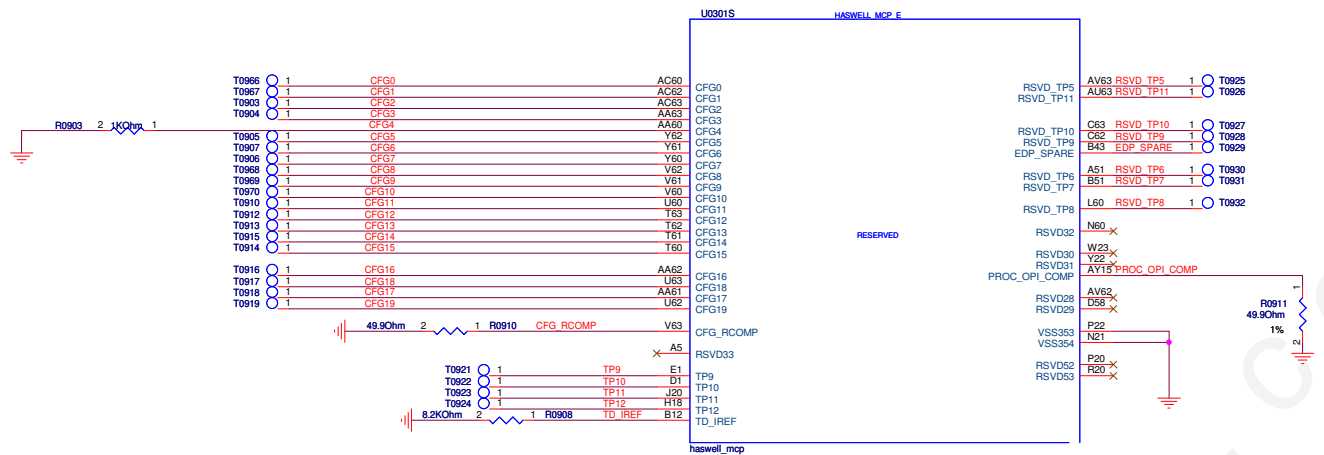


X750LB/LA with Shark Bay ULT

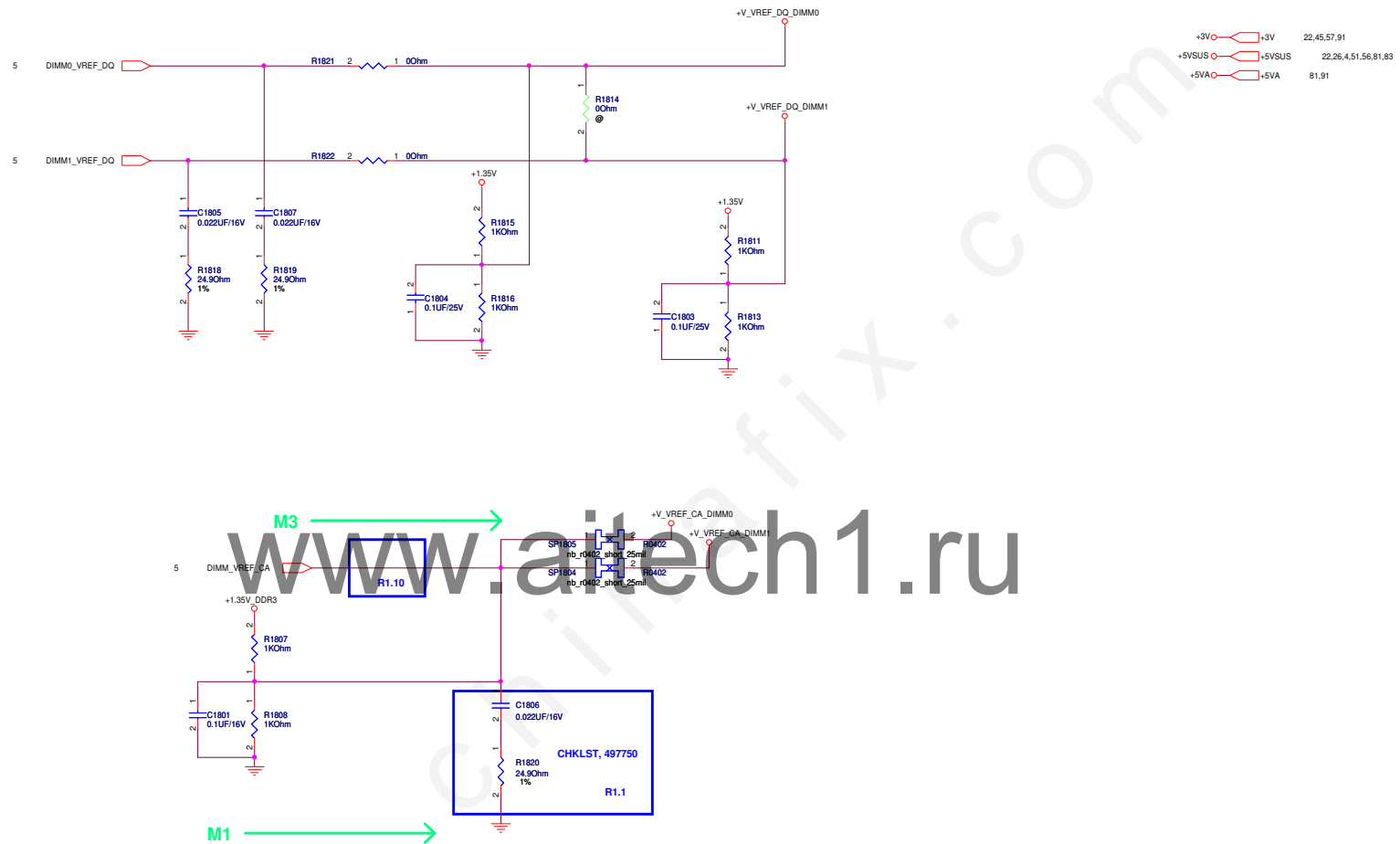
BLOCK DIAGRAM

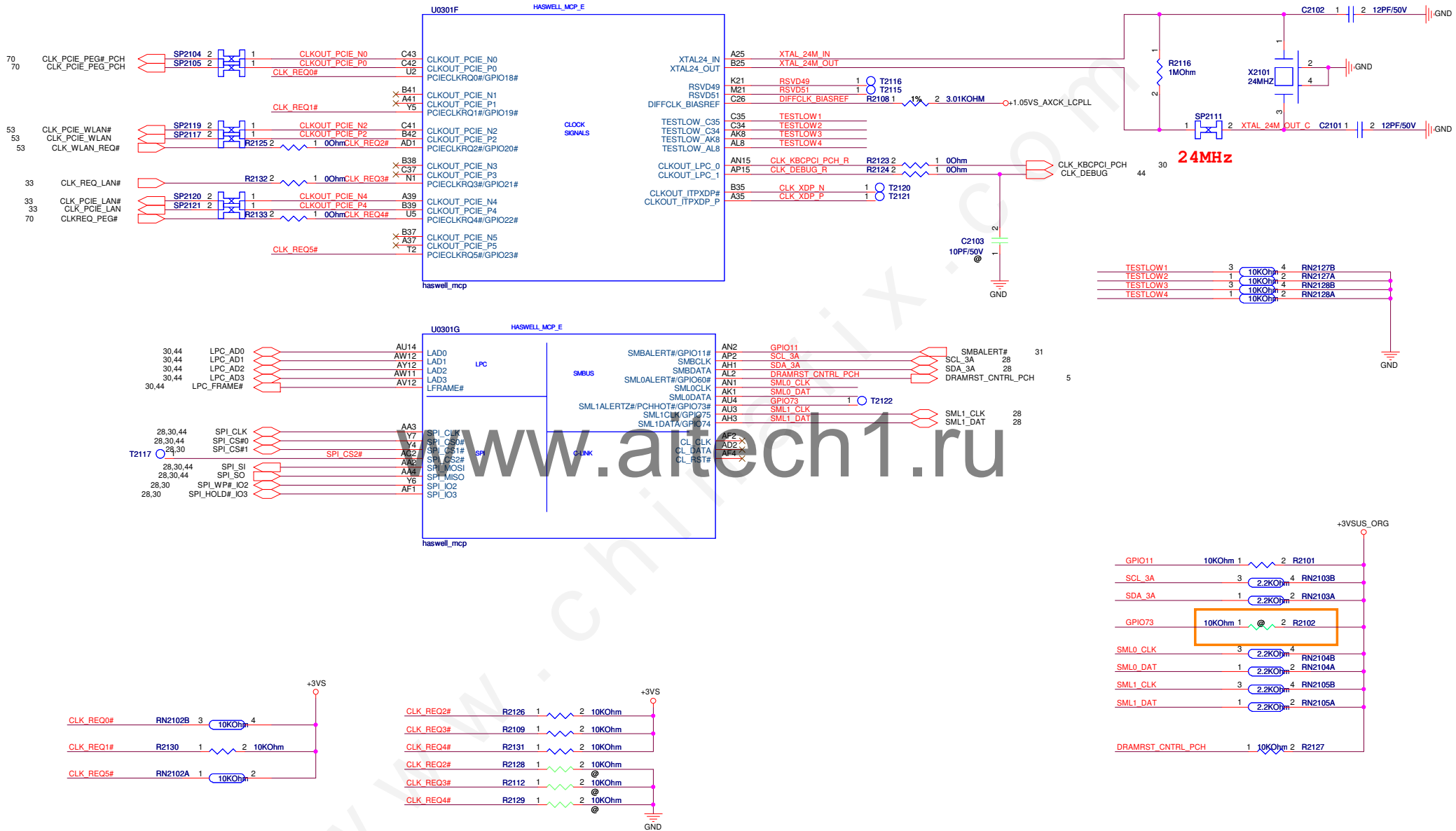


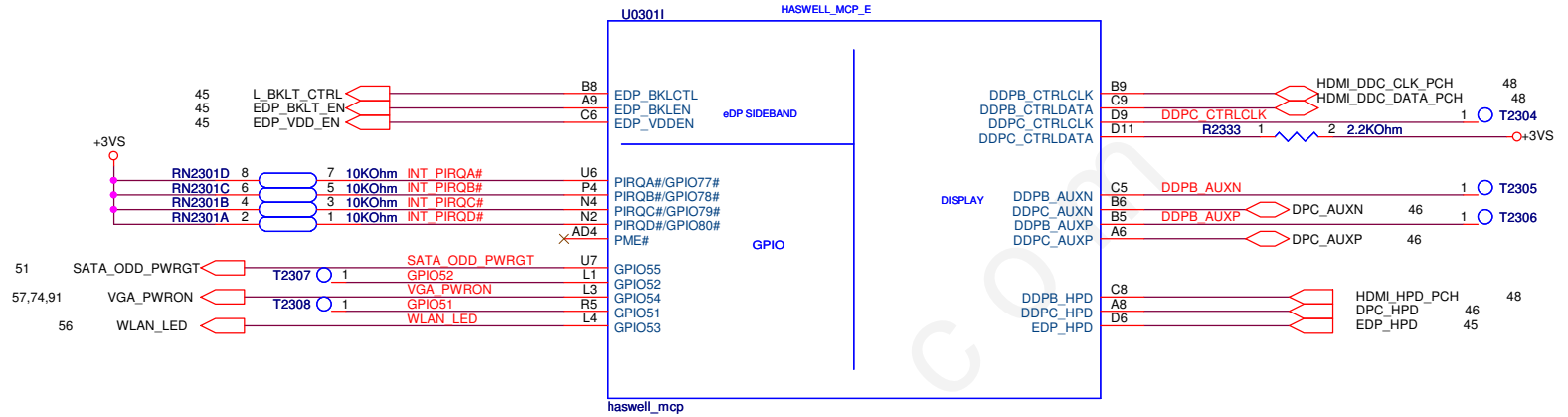
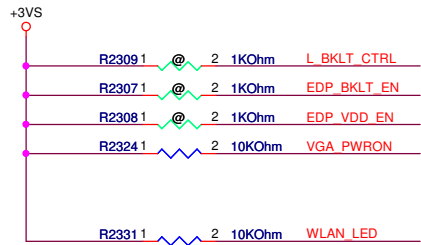




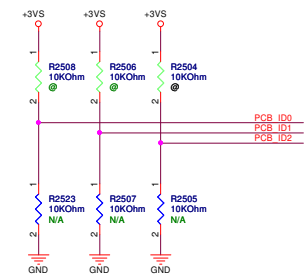
DDR3 Vref





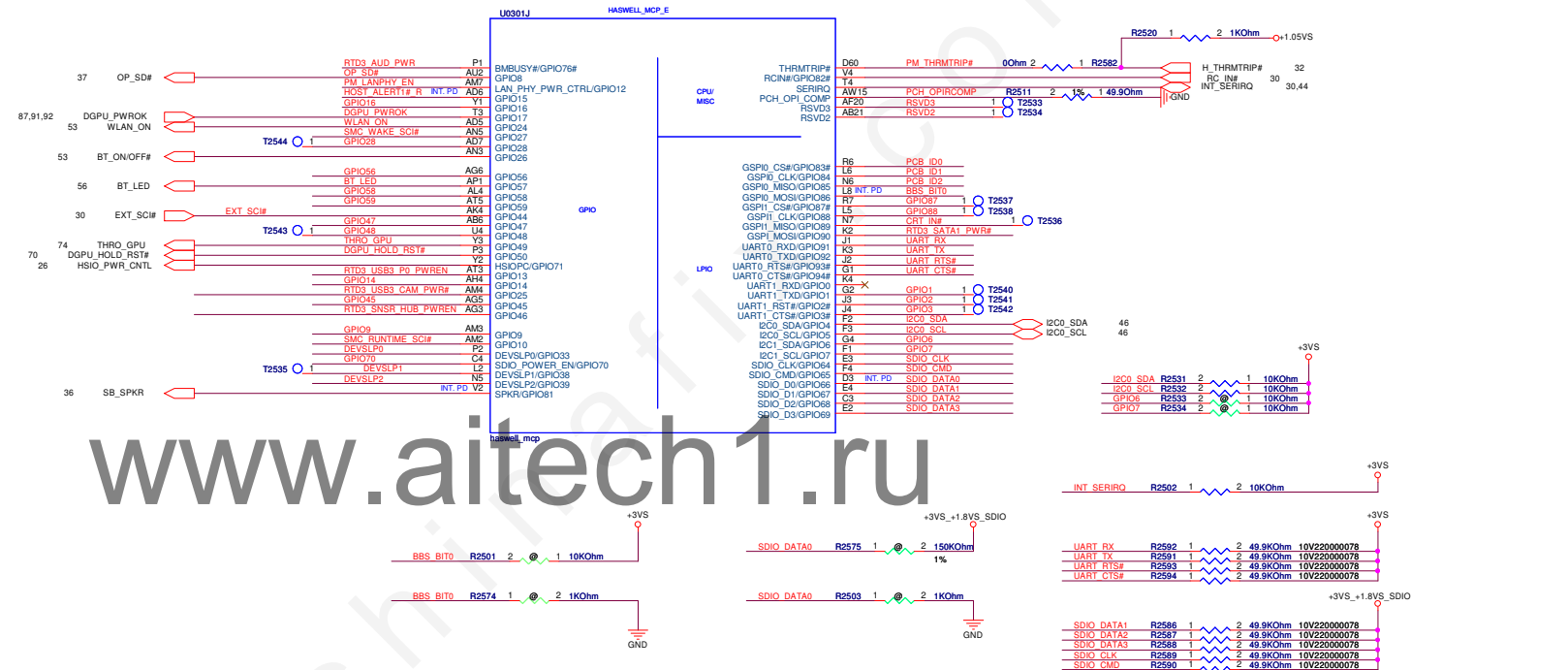
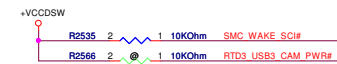
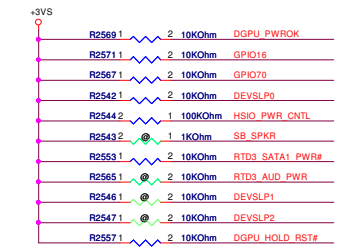
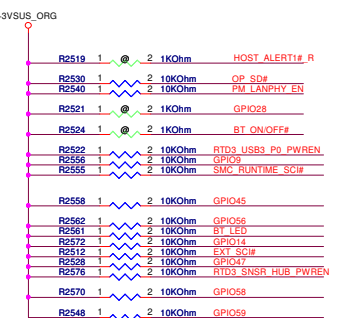


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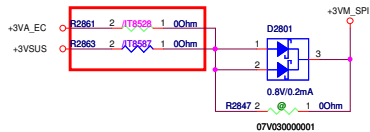
BIOS Rev. SKU

ID0	ID1	ID2	PCB Rev.
0	0	0	TBD
1	0	0	TBD
0	1	0	TBD
1	1	0	TBD
0	0	1	TBD
1	0	1	TBD
0	1	1	TBD
1	1	1	TBD



PCH SPI ROM

+3VA_EC reserved for share ROM



IT8587 mirror code

EC與SPI ROM的power plane需相同

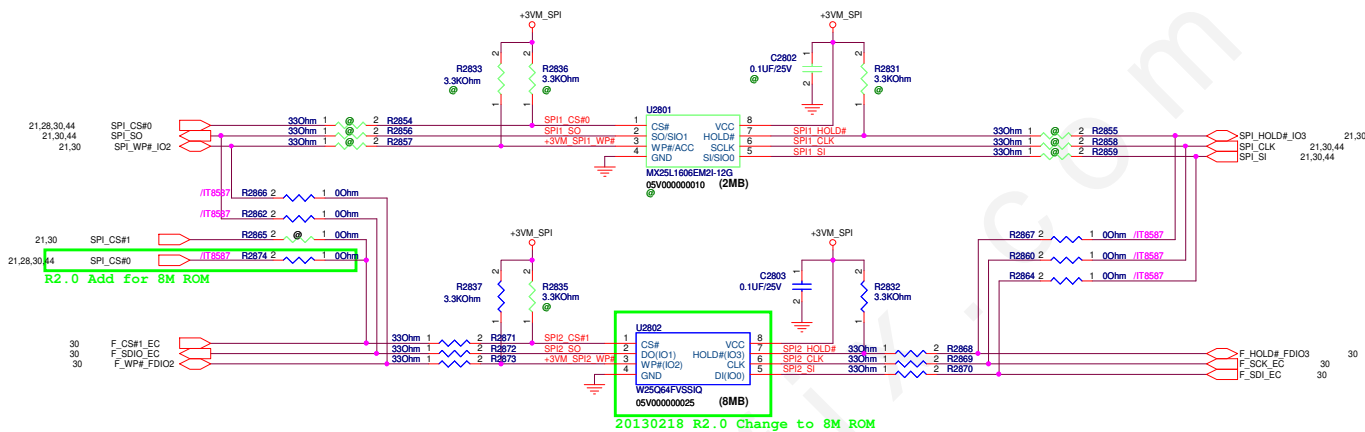
Option for Win8

Configuration1(Win 7)

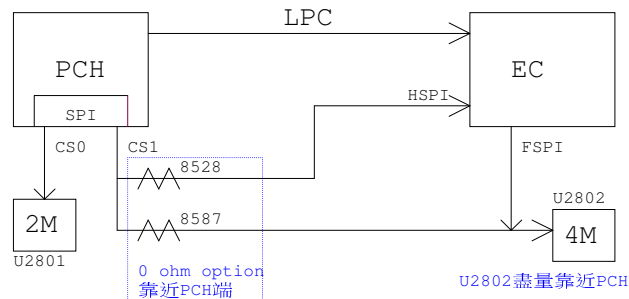
U2801	@	
U2802	@	
U2803	ME+BIOS+EC	4MB
ummount:	R2855, R2856, R2864, R2865, R2853, R2852, R2834, R2850, R2851, R2832, C2803, U2802, R2869, R2870, R2868, D2802, U2801, R2835, R2836	

Configuration2(Win 8)

U2801	ME Firmware	2MB
U2802	EC+BIOS	4MB
ummount:	R2858, R2862, R2866, R2867, U2803	



EC co-lay 8528/8587 SPI Structure

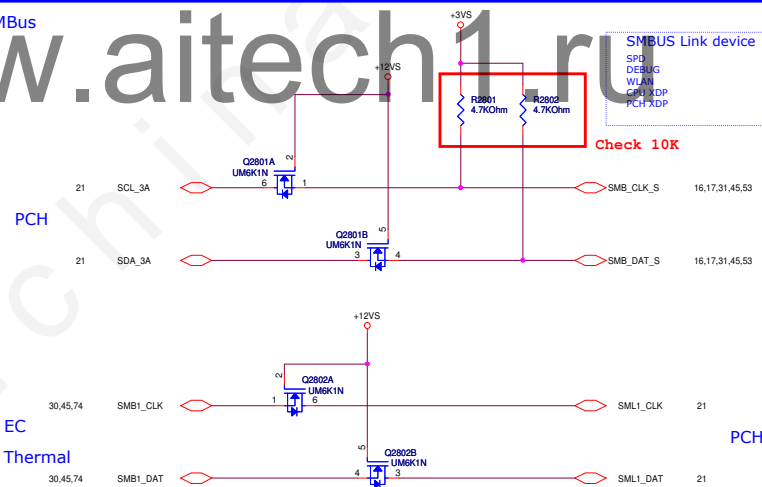


PCH SMBus

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PCH

EC VGA Thermal



PEGATRON Title : PCH(9)_SPI,SMB

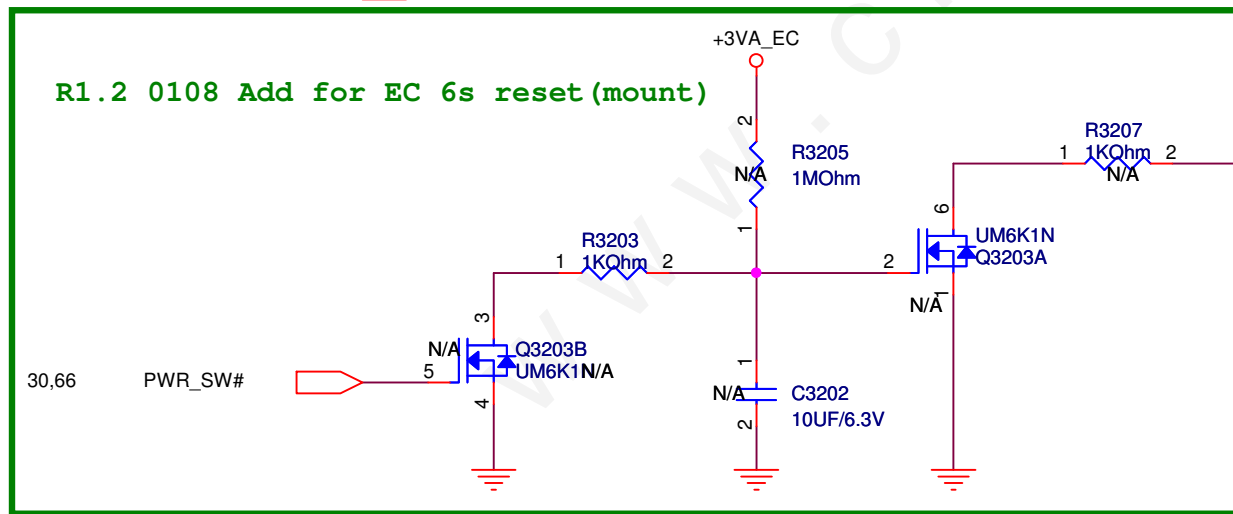
Size	Project Name	Rev
C	X750LB	1.1
Date: Thursday, August 01, 2013	Sheet 26 of 100	

Thermal Policy

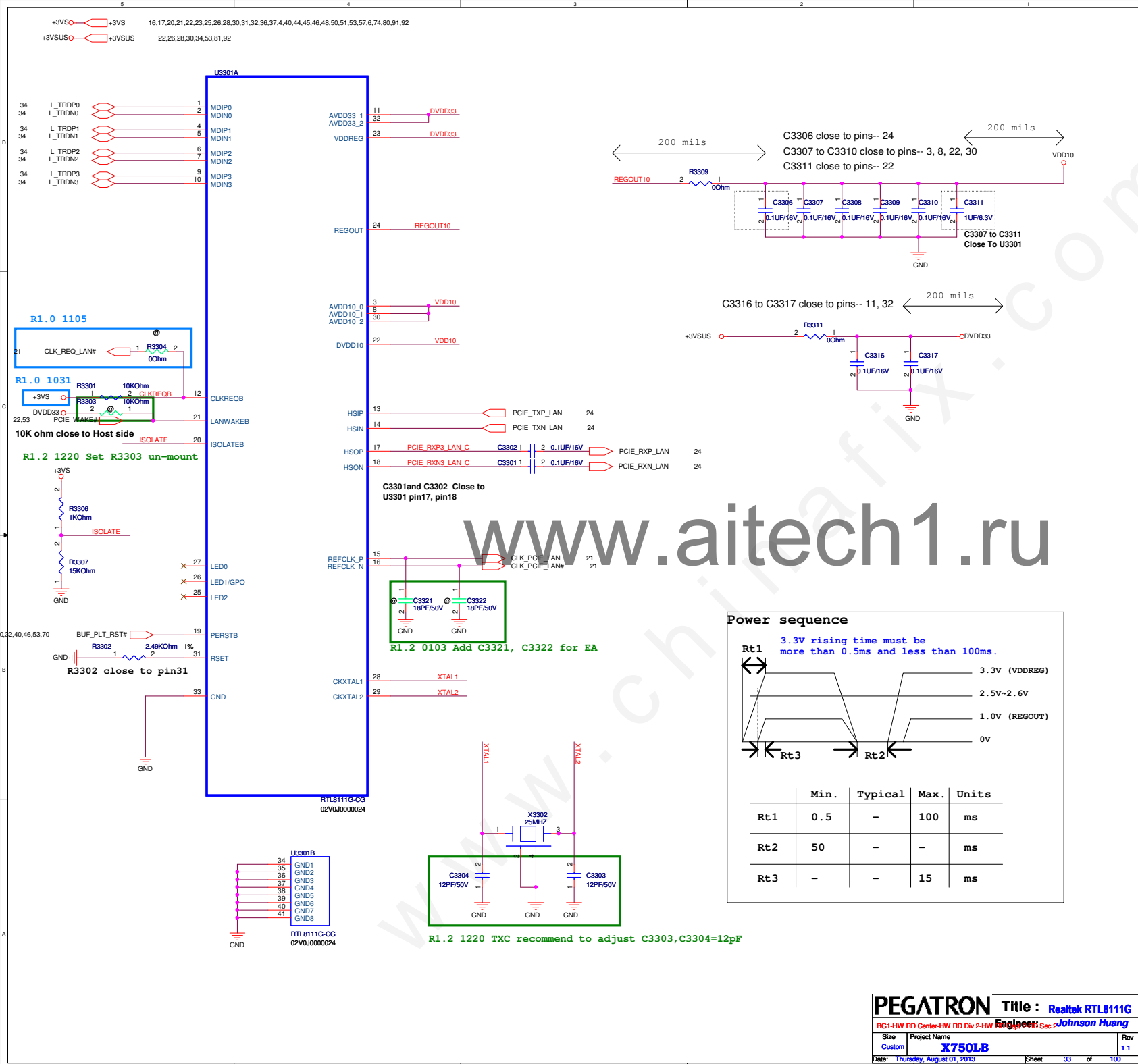
+3VS +3VA_EC +3VS +3VA_EC 16,17,20,21,22,23,25,26,28,30,31,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92 28,30,44,66

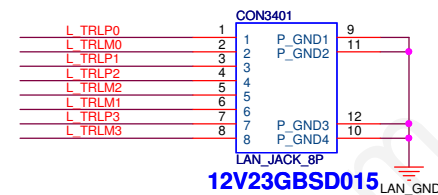
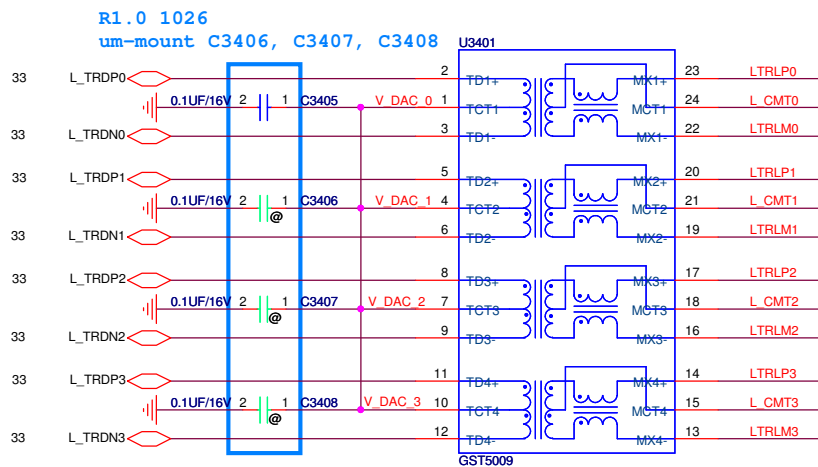
**NPCE795 has internal power-on reset circuit
Use 47k ohm to make sure that raising time of
POR is less than 10us**

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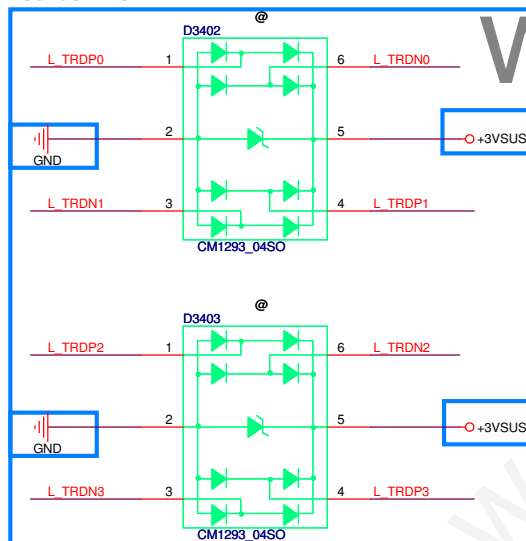
PEGATRON		Title : RST_Reset Circuit	
		Engineer: Johnson Huang	
Size A	Project Name X750LB		Rev 1.1
Date: Thursday, August 01, 2013		Sheet 32 of 100	





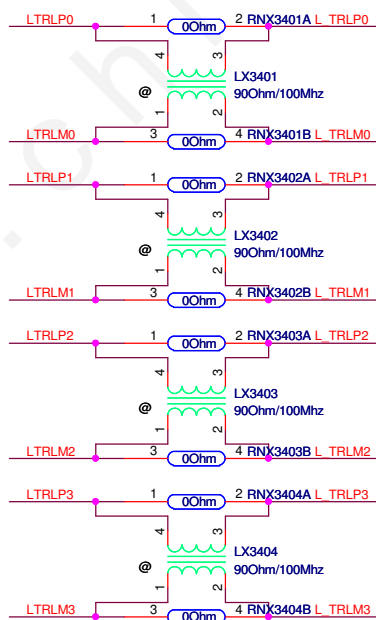
R1.0 1026 EMI

建議將TVS (D3402, D3403) 放置在一出transformer往chip方向的位置,
change net define

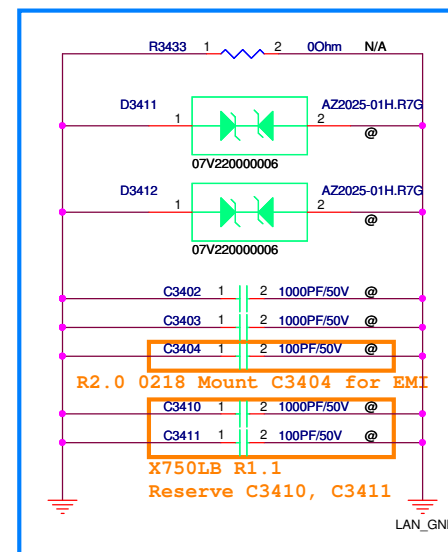


R1.0 1031 change power rail of D3402, D3403

R1.0 1105 change LAN_GND to GND

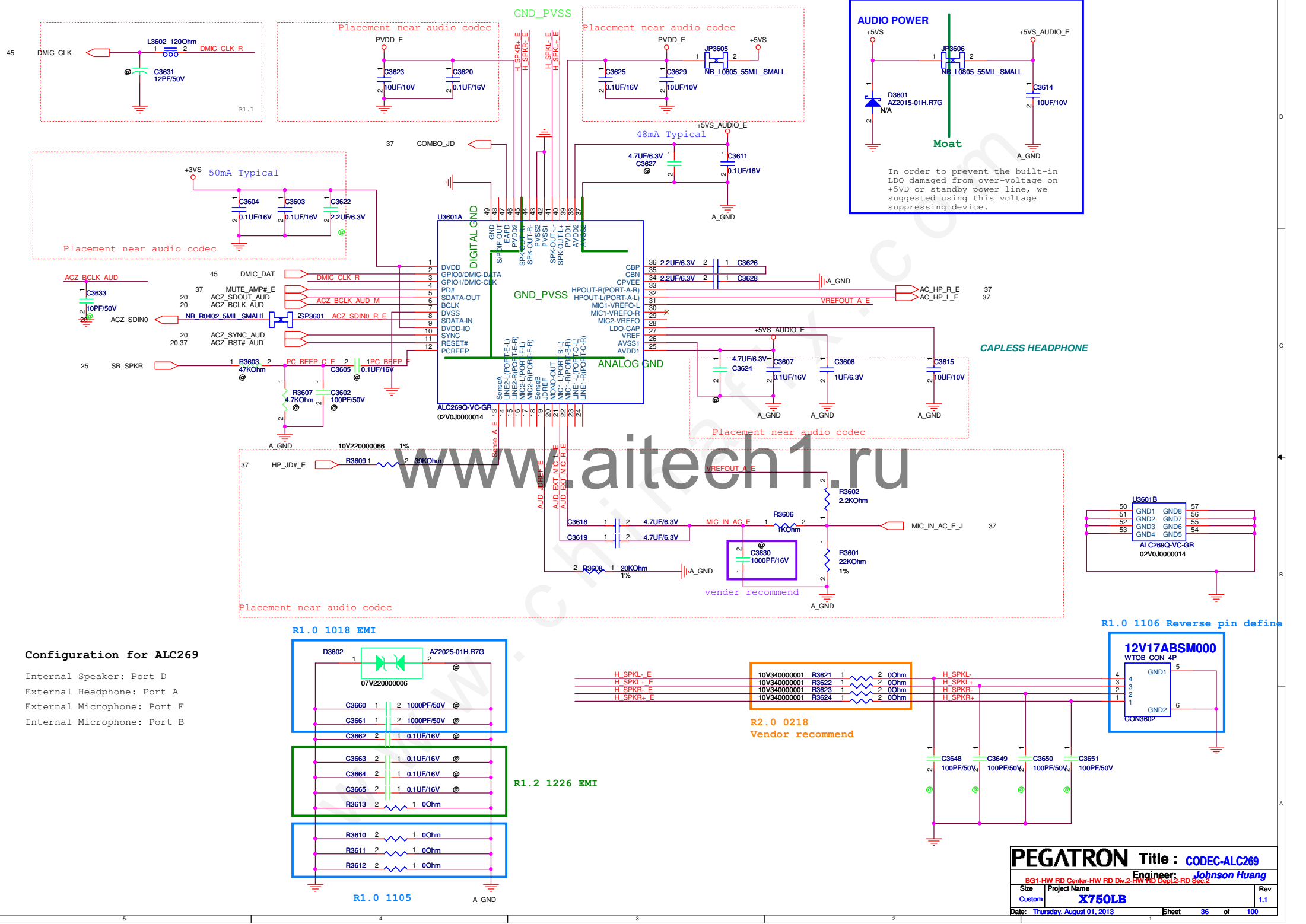


R1.0 1018 EMI



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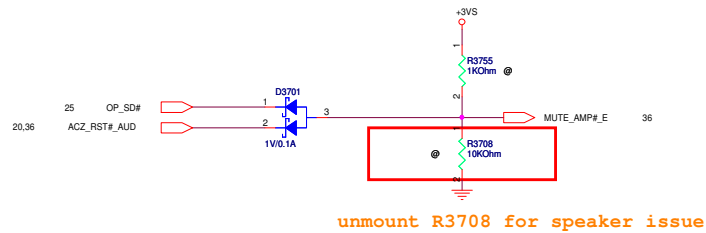
PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD		Engineer: Johnson Huang	
Size C	Project Name X750LB		Rev 1.1
Date: Thursday, August 01, 2013		Sheet	35 of 100



Configuration for ALC269

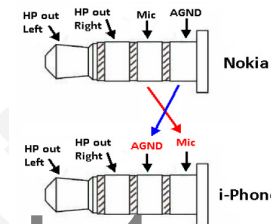
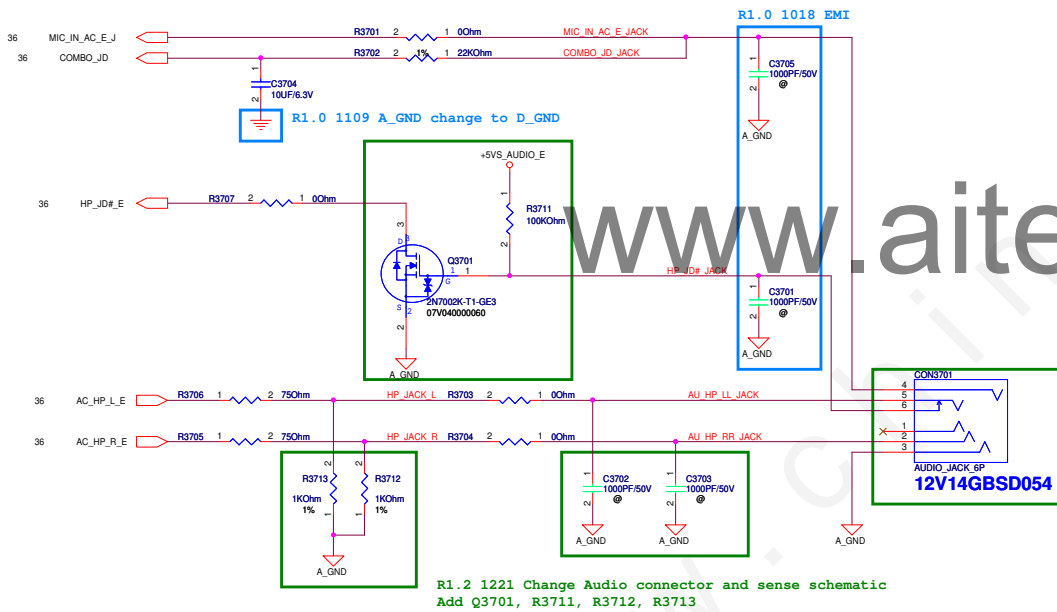
- Internal Speaker: Port D
- External Headphone: Port A
- External Microphone: Port F
- Internal Microphone: Port B

AMP De-Pop Control circuit



Moat D_GND
A_GND

HP/MIC Combo JACK (for i-Phone only)



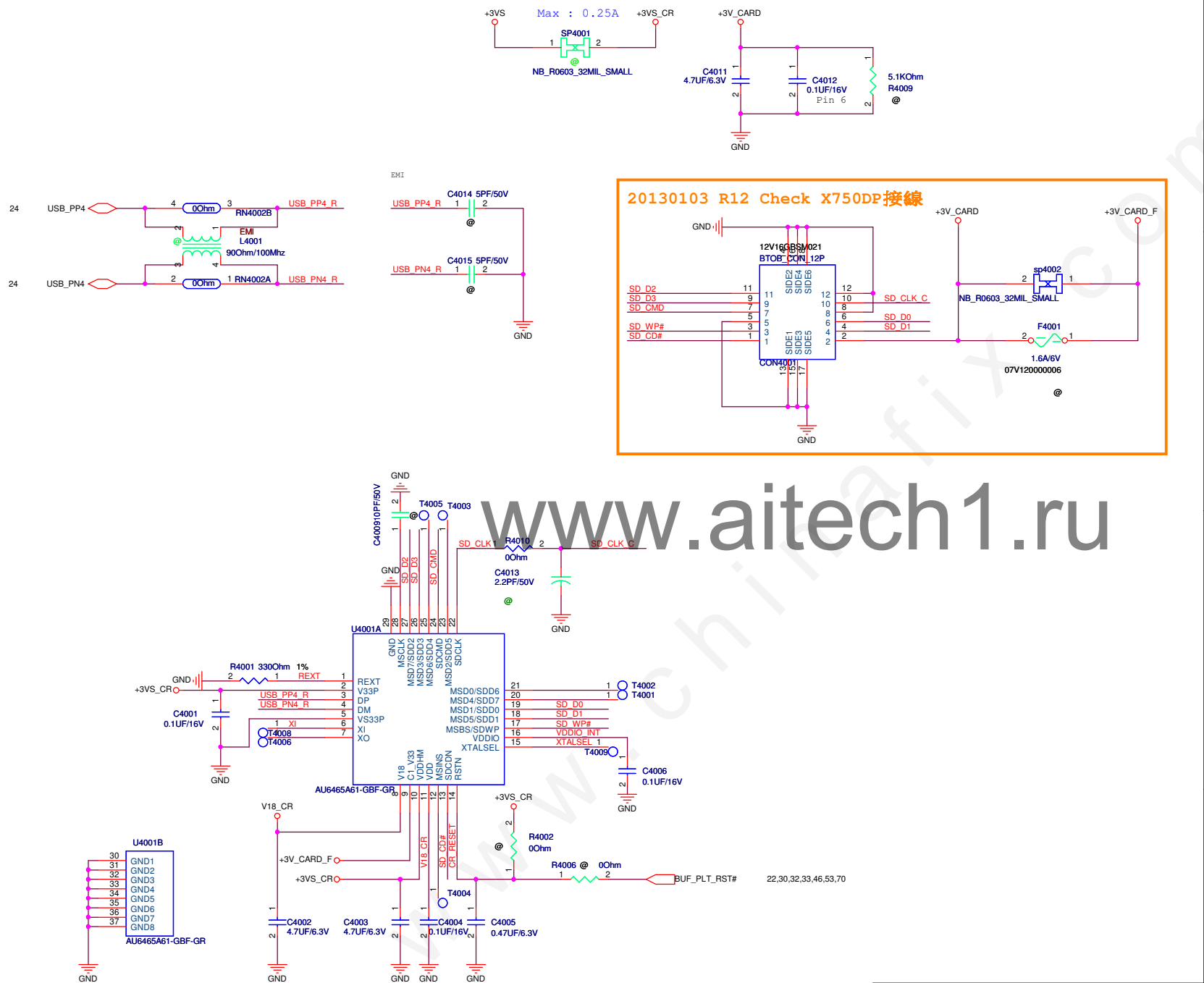


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Title			
<Title>			
Size	Document Number		Rev
A	X750LB		1.1
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Title			
<Title>			
Size	Document Number		Rev
A	X750LB		1.1
Date:	Thursday, August 01, 2013	Sheet	39 of 100



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PEGATRON		Title : AU6465	
BG1HW5W		Engineer:	
Size	Project Name	X750LB	Rev 2.1
Custom			
Date: Thursday, August 01, 2013		Sheet 40	of 104

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PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	41 of 100

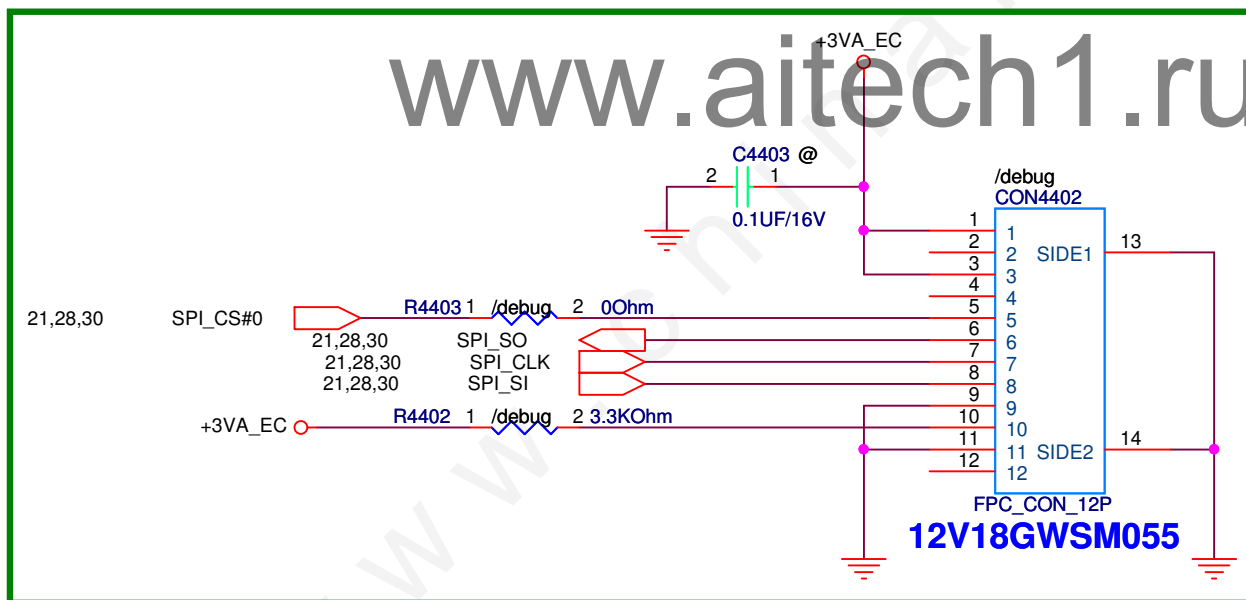
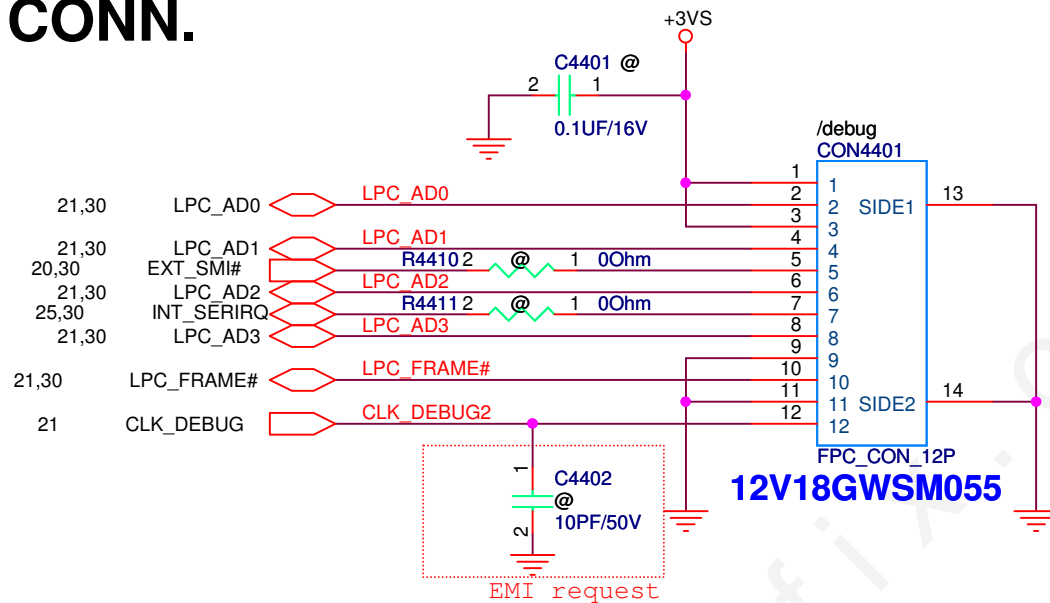
www.aitech1.ru

PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	42 of 100

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PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	43 of 100

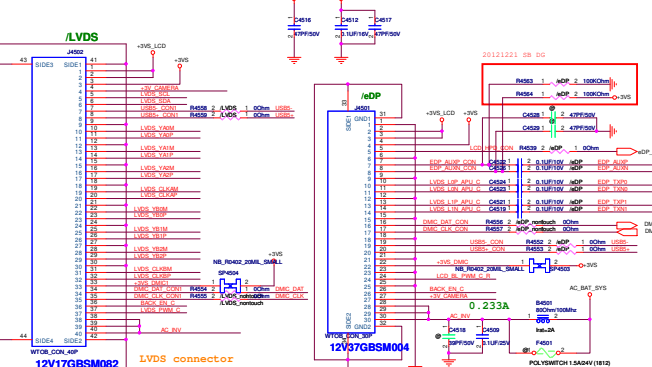
DEBUG CARD CONN.



R1.2 1220 Change the connection of CON4402
from U2802 (BIOS) to U2801 (ME)

PEGATRON		Title : DEBUG CONN.	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2-HW RD Ser.2		Engineer: Johnson Huang	
Size A	Project Name X750LB		Rev 1.1
Date: Thursday, August 01, 2013		Sheet 44	of 100

LVDS Conn w/Camera Module



LVDS connector 12V17GBSM082
M:1217-00V9000
S:1237-0000000

LVDS connector 12V37GBSM082
M:1237-002A000
S:1237-002E000

LVDS_VCC for eDP
From PCH 25 EDP_VDD_EN
From LVDS chip LVDS_ENVDD

LVDS_VCC for LVDS
LVDS_ENVDD
LVDS_VDD

1109 R10 add DMIC only conn.



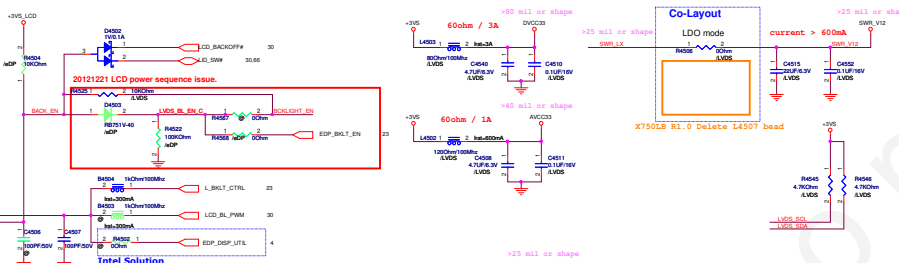
Touch panel



12V17GBSM090

CON4502 & C4519 EN 100mA

Controller circuit



20121221 SW 10

From CPU

From SC

For RTD1368 CONF1G

For RTD1338 CONF1G

For RTD1368 CONF1G

For RTD1338 CONF1G

For RTD1368 CONF1G

For RTD1338 CONF1G

For RTD1368 CONF1G

For RTD1338 CONF1G

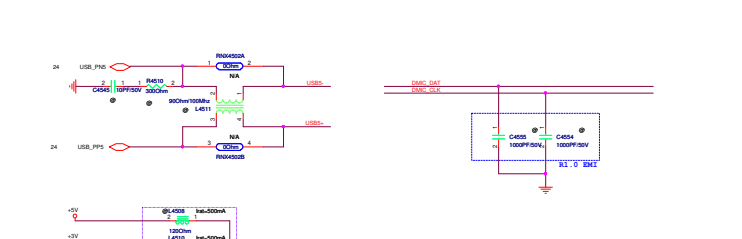
For RTD1368 CONF1G

For RTD1338 CONF1G

For RTD1368 CONF1G

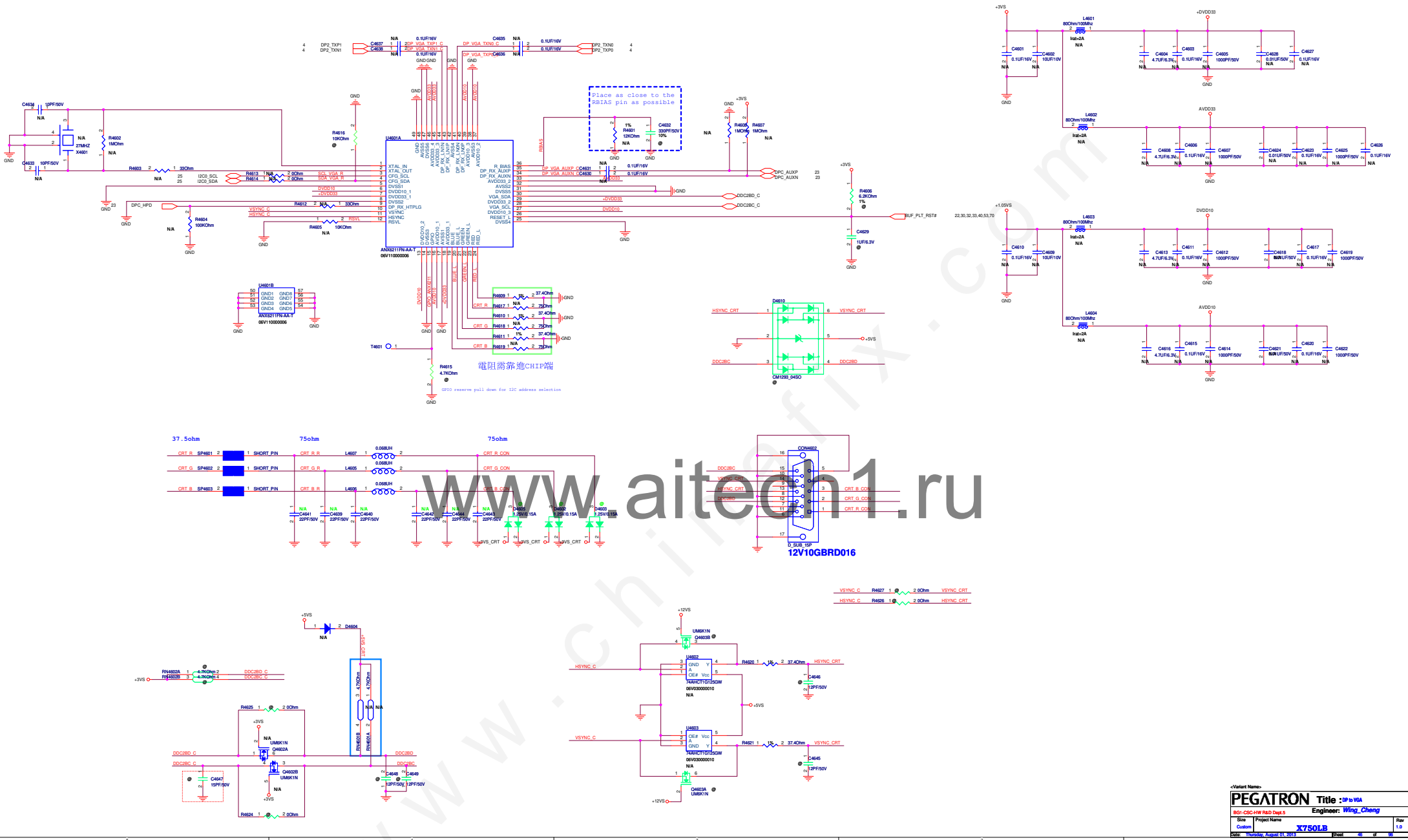
For RTD1338 CONF1G

D-Mic + Camera



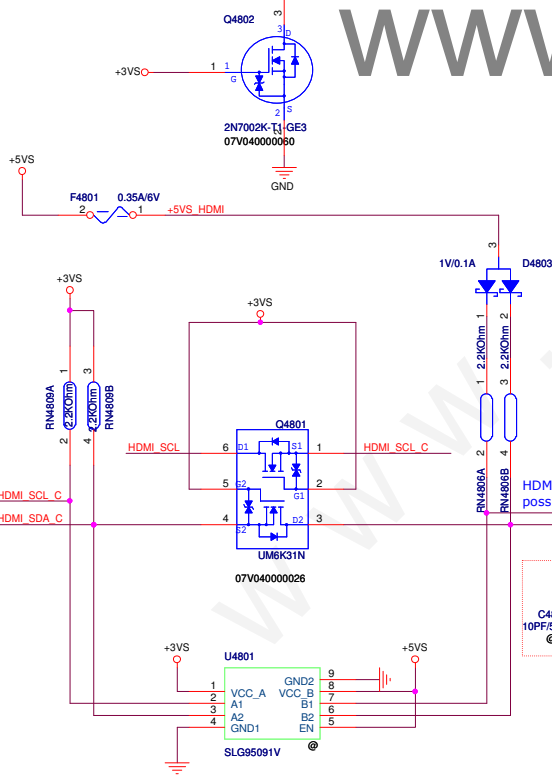
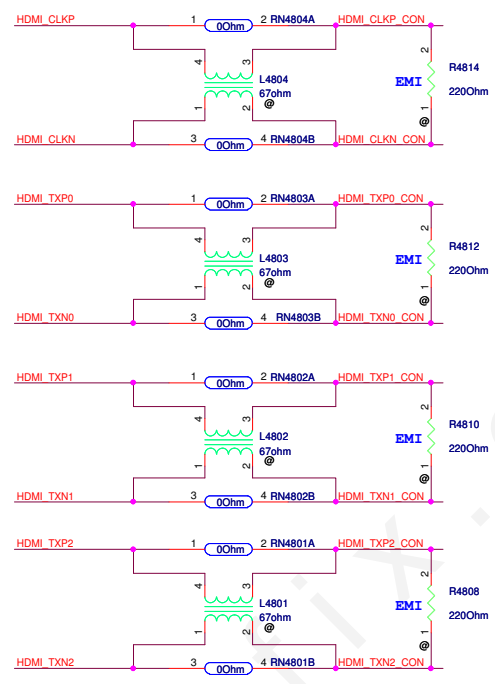
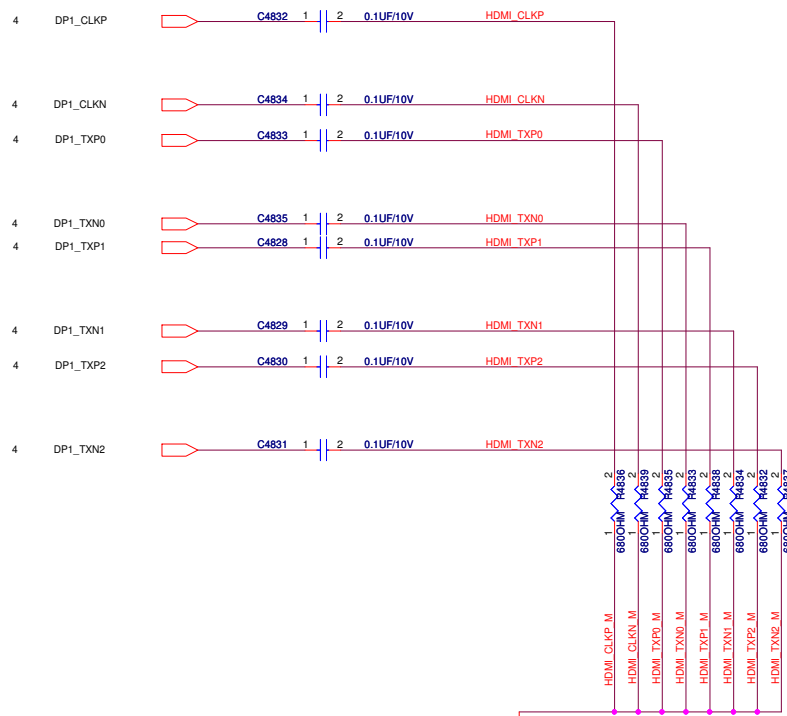
12V17GBSM090

CON4502 & C4519 EN 100mA



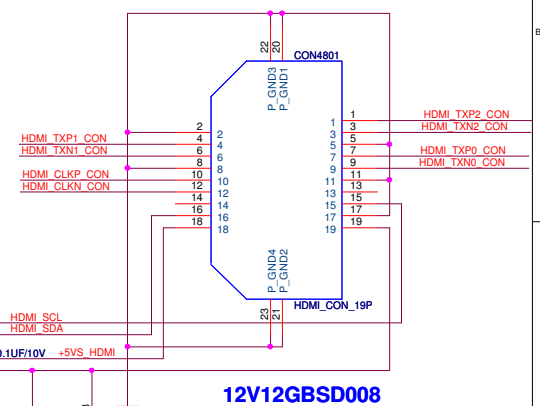
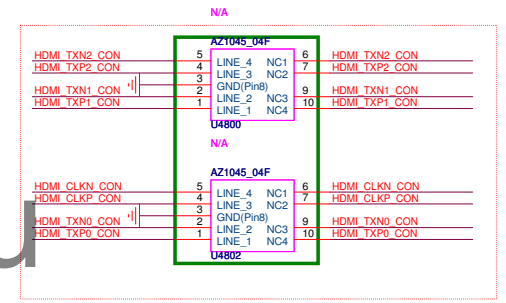
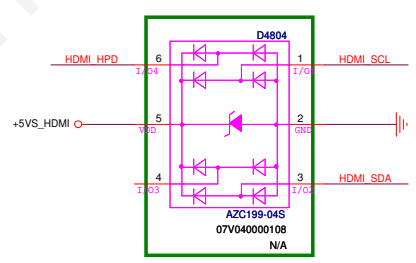
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PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
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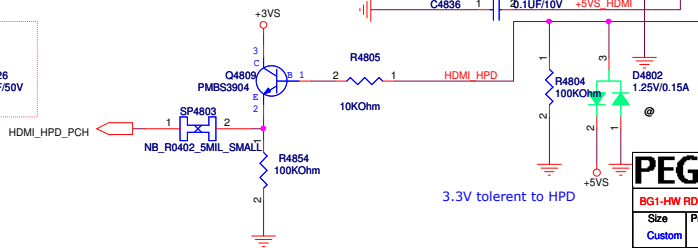
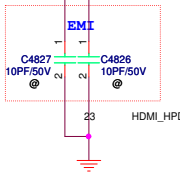


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R1.2 0108 Mount D4804, U4800, U4802 for EMI



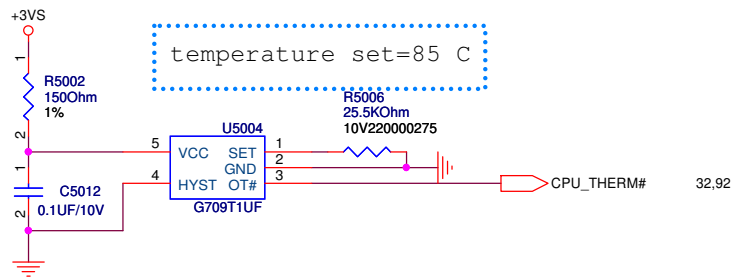
12V12GBSD008



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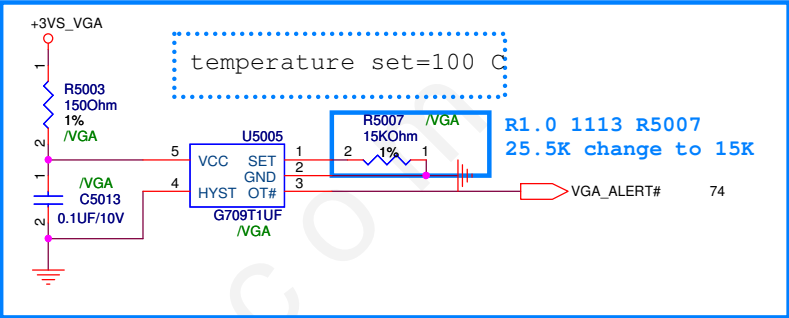
PEGATRON		Title : HDMI CEC	
BG1-HW RD Center-HW RD Div.2-HW RD Supp.15 Rev.2		Engineers Johnson Huang	
Size Custom	Project Name X750LB		Rev 1.1
Date: Thursday, August 01, 2013		Sheet	49 of 100

CPU Thermal Sensor

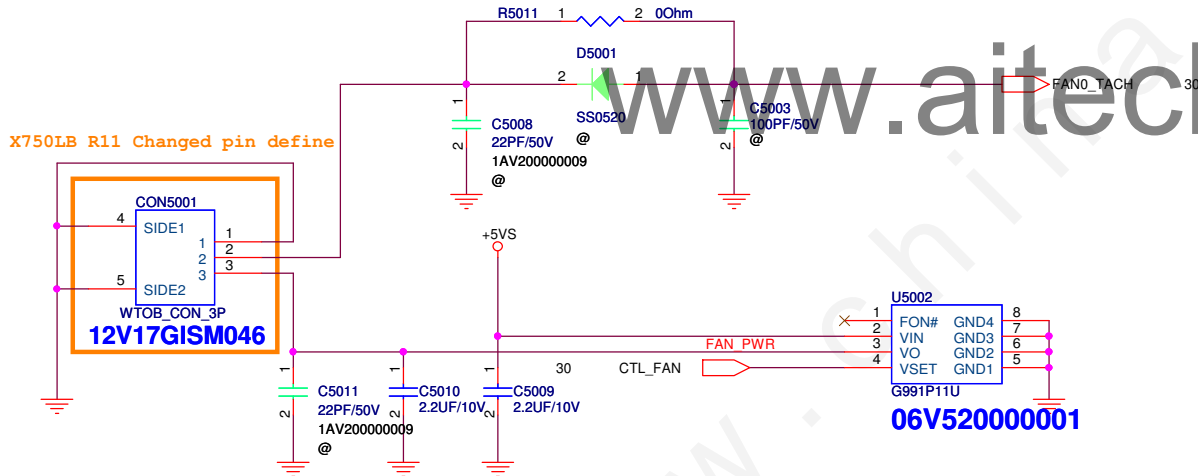


GPU Thermal Sensor

R1.0 1031 Thermal Request (ABBA DFA)

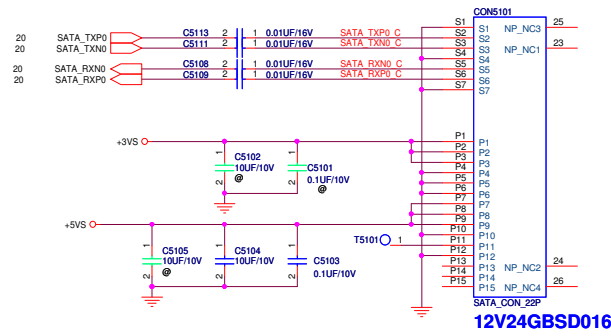


FAN

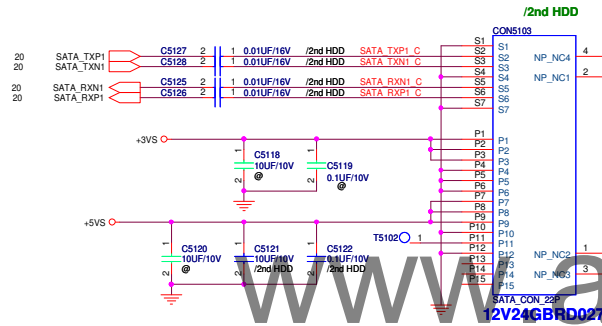


PEGATRON		Title : <i>FAN / Thermal Sensor</i>	
		Engineer: <i>Johnson Huang</i>	
Size	Project Name	X750LB	Rev 1.1
Custom			
Date: <i>Thursday, August 01, 2013</i>		Sheet <i>50</i> of <i>100</i>	

HDD

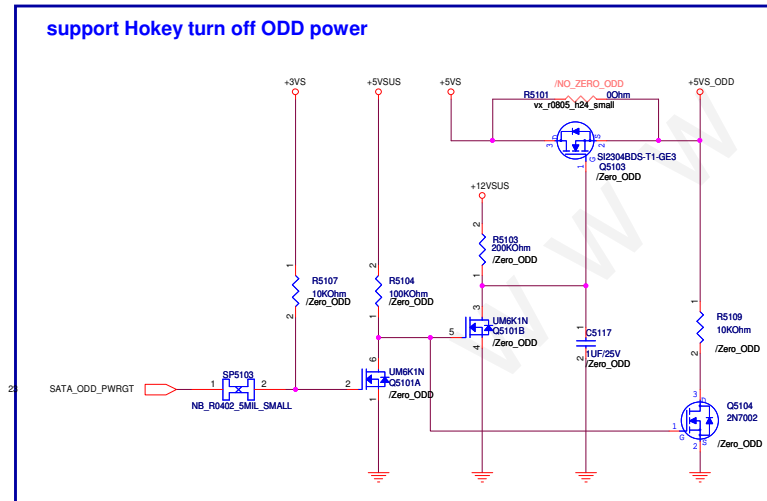


2nd HDD

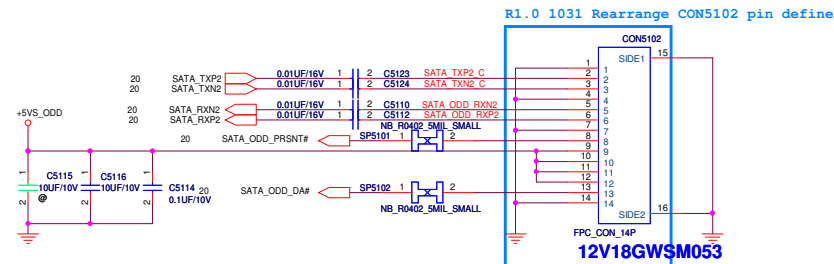


ZERO POWER ODD SUPPORT

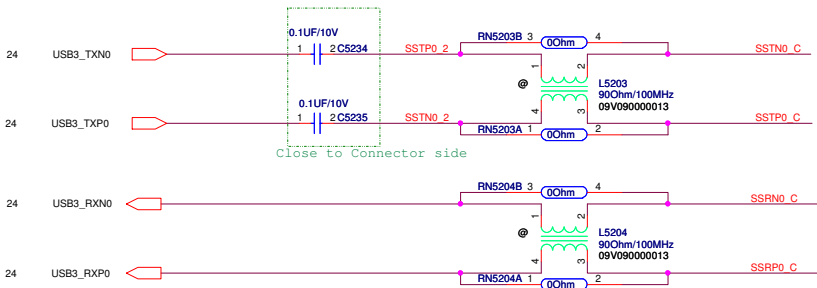
support Hokey turn off ODD power



ODD



Left USB3.0



Sleep & Charge (only 1 pcs)

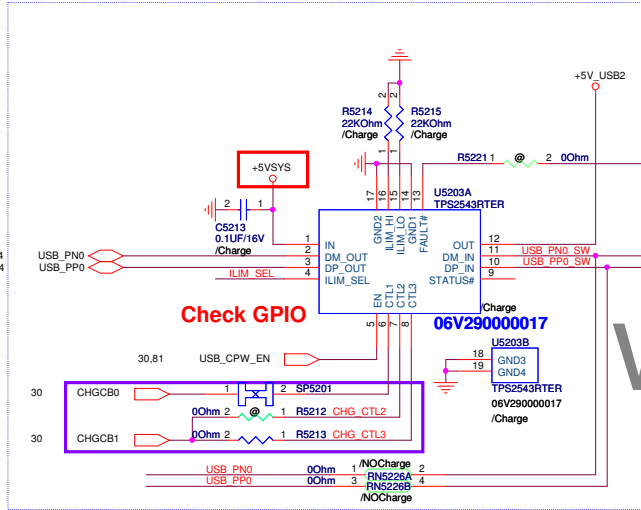
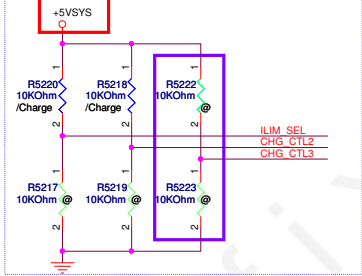
TPS2543

Check truth table

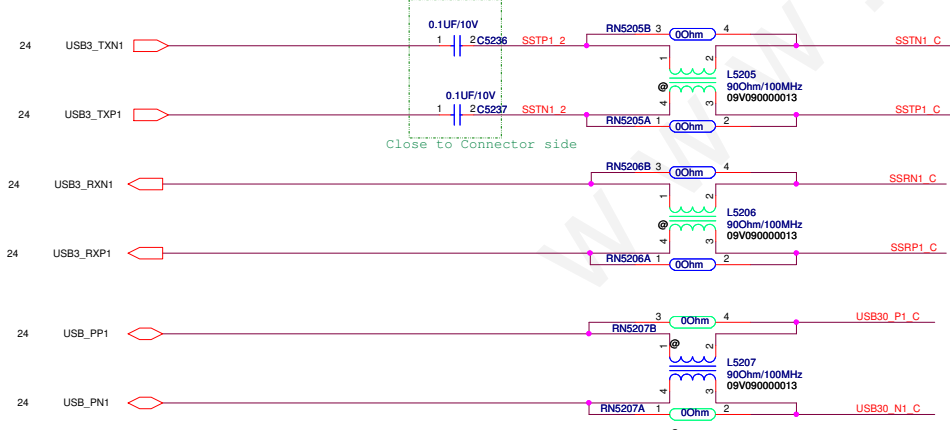
* ILIM_SEL = H, CHG_CTL3 = H

CTL1	CTL3	FUNCTION
0	1	Auto mode
1	1	CDP mode

MODE SELECT

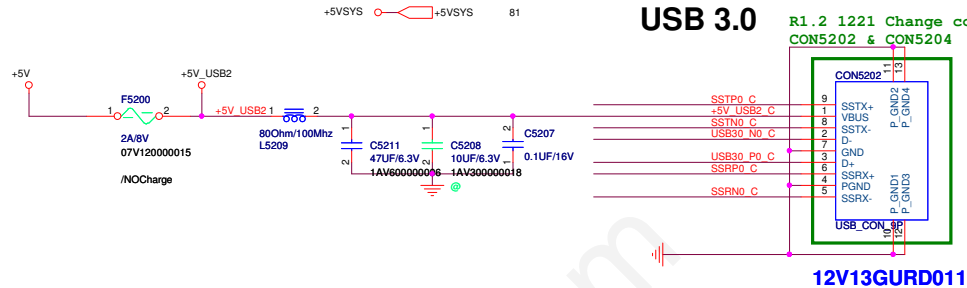


X750LB R11 modify for USB Charger issue



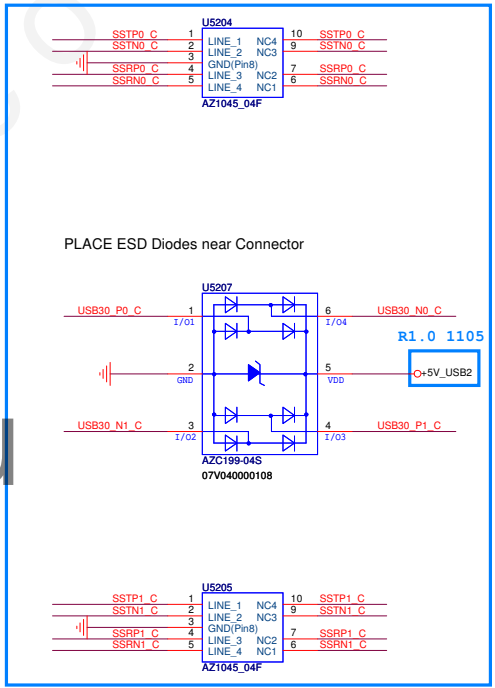
USB 3.0

R1.2 1221 Change connector CON5202 & CON5204

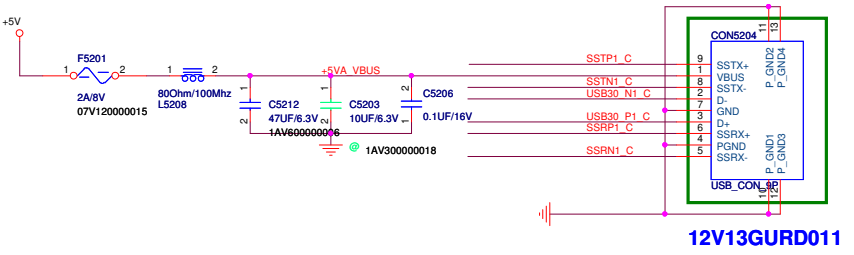


12V13GURD011

R1.0 1018 EMI

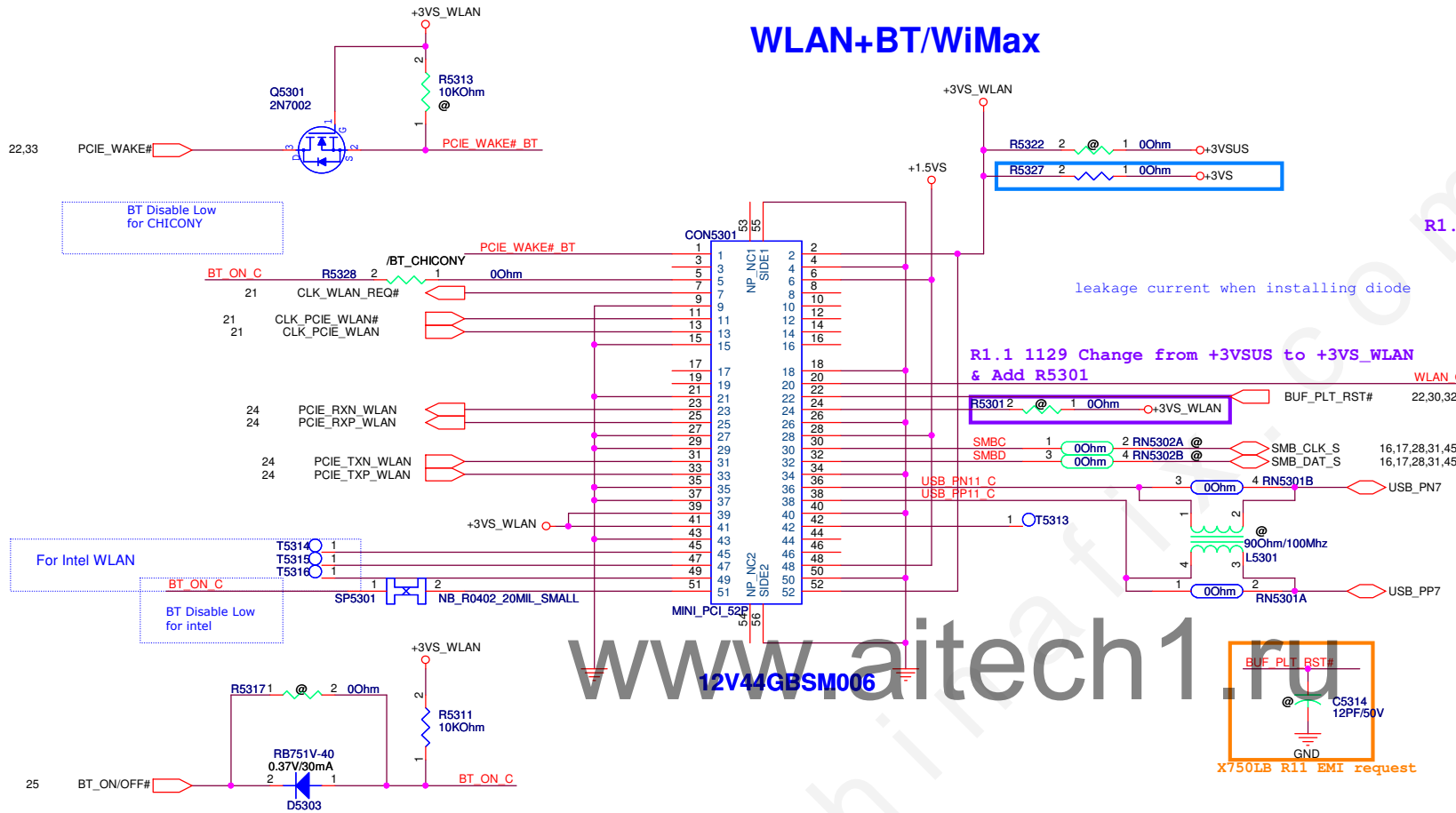


USB 3.0

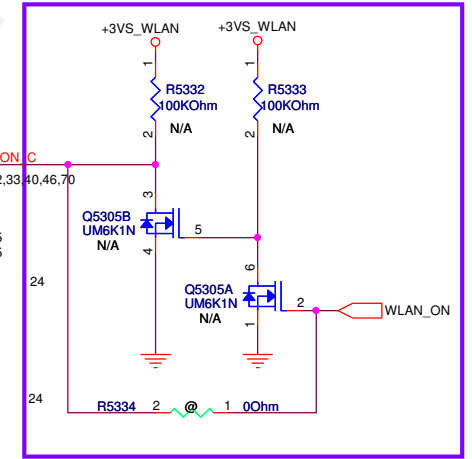


12V13GURD011

WLAN+BT/WiMax



R1.0 1129 mount MOS and um-mount 0 ohm.

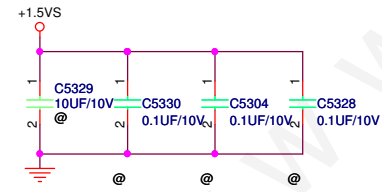


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H = 6.5 mm

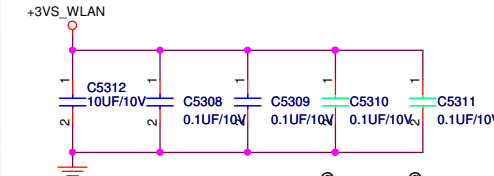
WLAN +1.5VS bypass capacitor:

Place 0.1uF near pin 6,28,48.
Place 10uF near +1.5VS source side.



WLAN +3VS bypass capacitor:

Place 0.1uF near pin 2,24,52,39 41.
Place 10uF near +3VS_WLAN source side.









PEGATRON		Title : MINICARD WLAN	
BG1-HW RD Center-HW RD Div.2-HW RD Center RD		Engineer: Johnson Huang	
Size B	Project Name X750LB	Rev 1.1	
Date: Thursday, August 01, 2013		Sheet 53 of 100	

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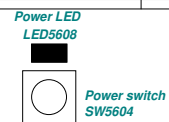
PEGATRON		Title : Mini Card	
BG1-HW RD Center-HW RD Div.2-HW RD Supp.10 Sec.2		Engineers Johnson Huang	
Size Custom	Project Name X750LB		Rev 1.1
Date: Thursday, August 01, 2013		Sheet	54 of 100

Camera

+3VS			+3VS	16,17,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+3V			+3V	22,45,57,91
+5V			+5V	45,52,57,66,91

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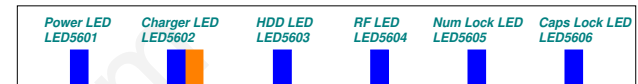
PEGATRON		Title : *****	
BG1-HW RD Center-HW RD Div.2-HW RD Dept. RD Sec.		Engineer: Johnson Huang	
Size A	Project Name X750LB		Rev 1.1
Date: Thursday, August 01, 2013		Sheet	55 of 100



Power Button

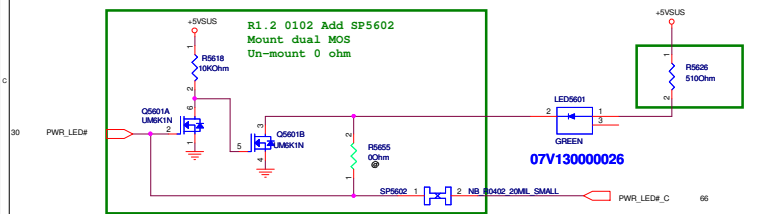
Wireless Button

LED Placement
Left-->Right

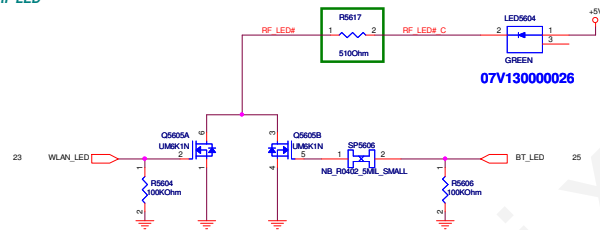


Power LED

R1.2 0108 Change all LED resistance = 510 ohm



RF LED

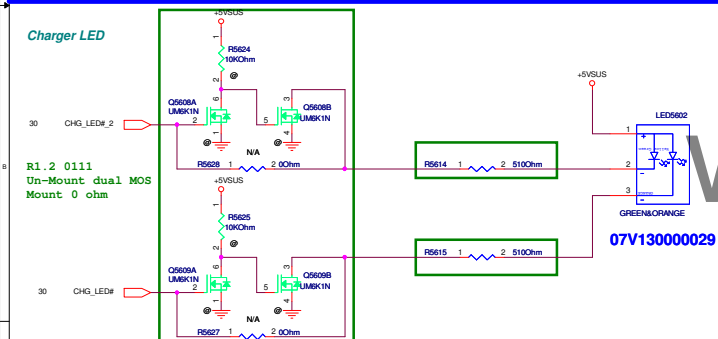


Charger LED

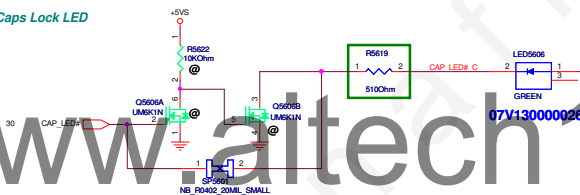
```

R1.2 0111
Un-Mount dua
Mount 0 ohm

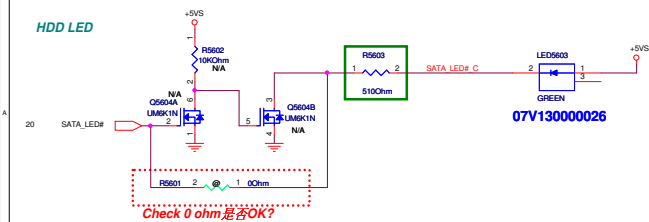
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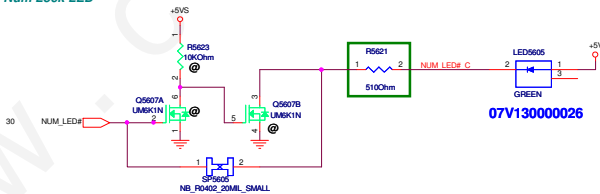
Caps Lock LED



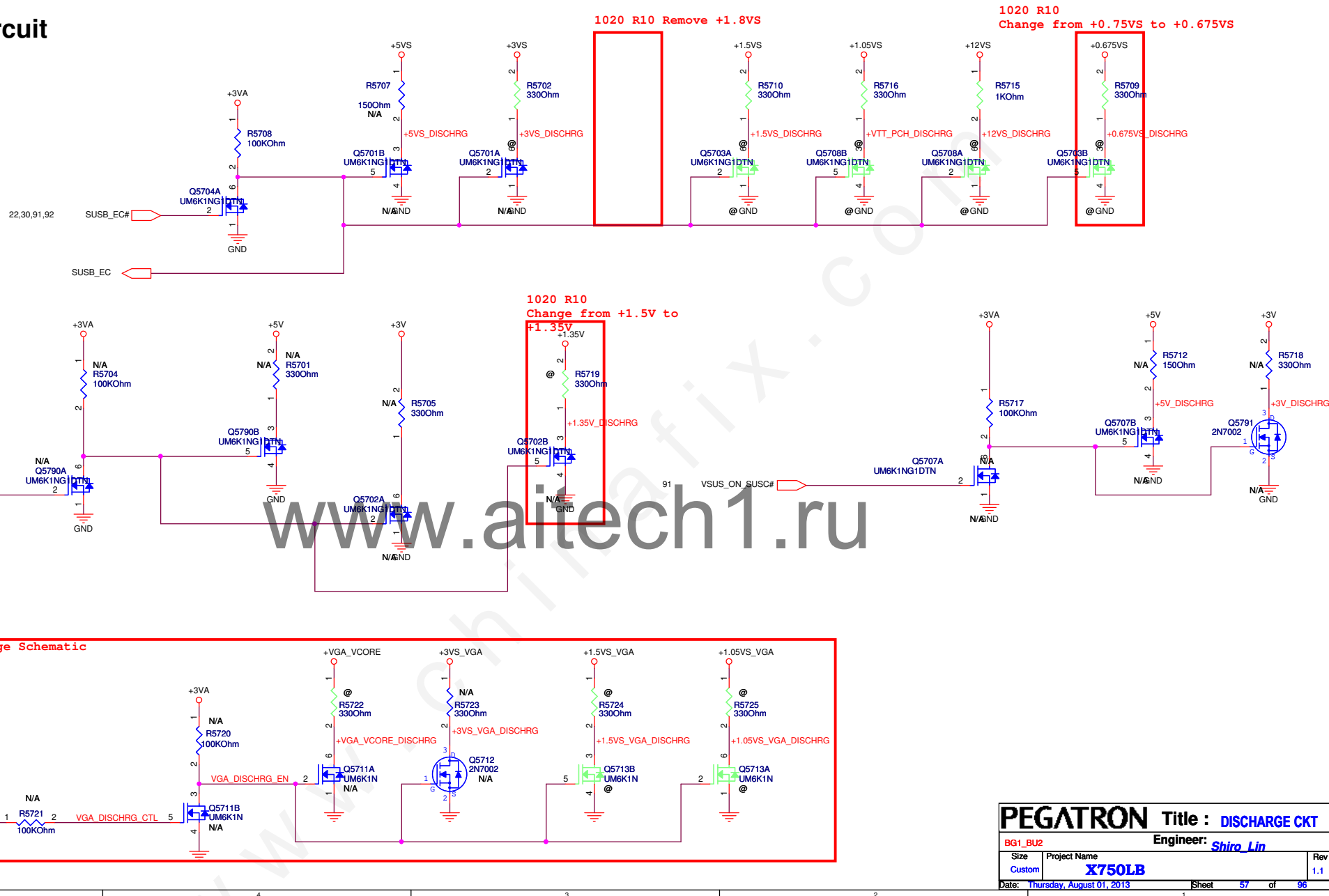
HDD LED



Num Lock LED



Discharge Circuit



PEGATRON		Title : DISCHARGE CKT	
BG1_BU2		Engineer: Shiro Lin	
Size Custom	Project Name X750LB		Rev 1.1
Date: Thursday, August 01, 2013		Sheet	57 of 96

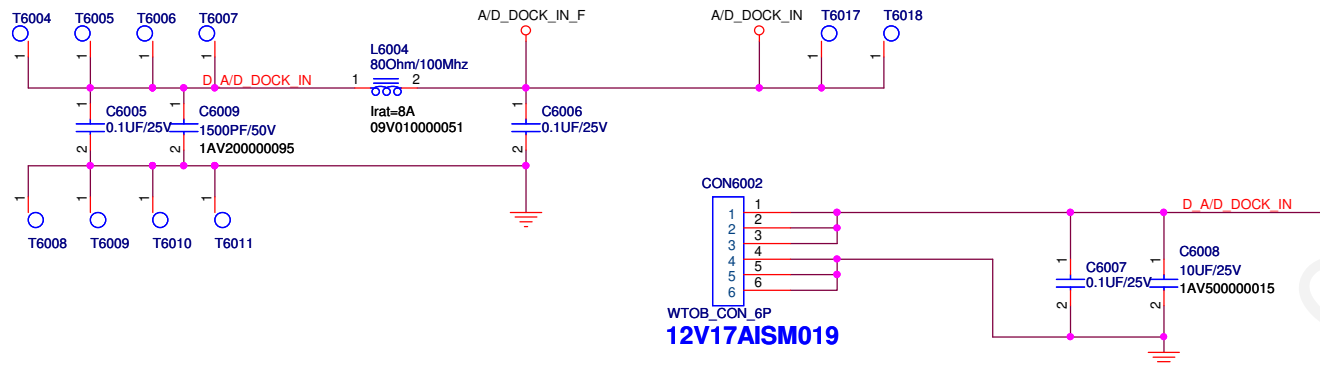
www.aitech1.ru

PEGATRON		Title : ASM1042	
BG1-HW RD Center-HW RD Div.2-HW RD		Engineer: Johnson Huang	
Size	Project Name		Rev
C	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	56 of 100

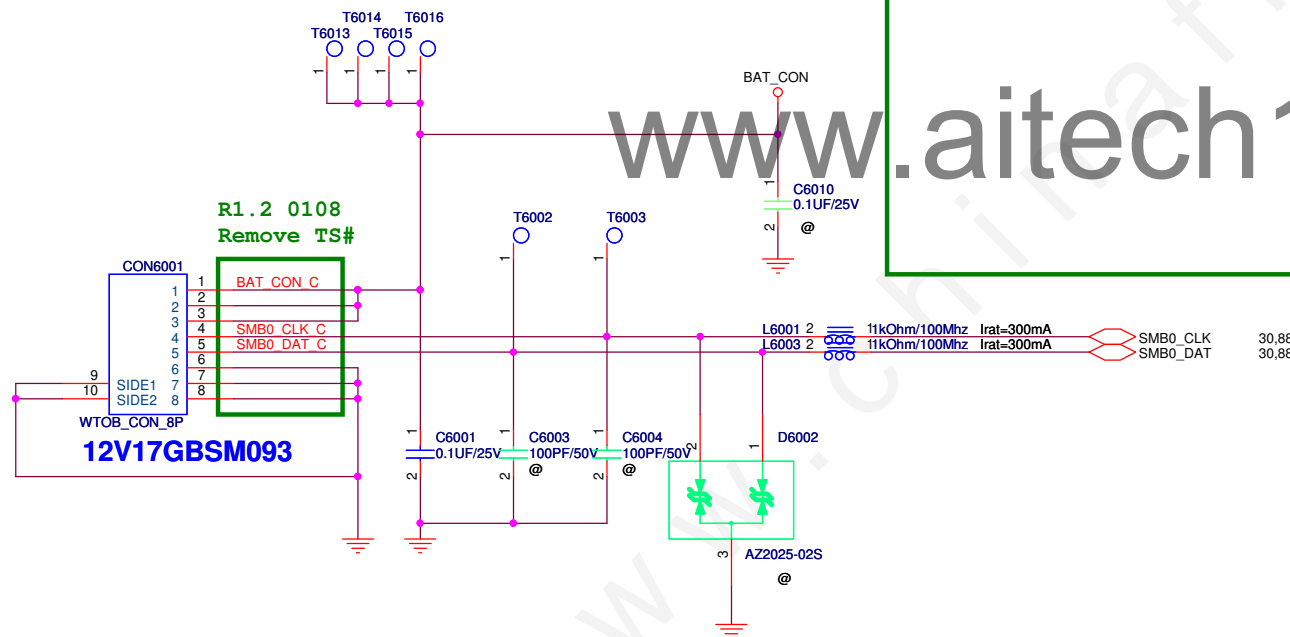
www.aitech1.ru

PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	59 of 100

DC IN



Battery Connector



R1.2 0108 Remove TS#



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PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	61 of 100

www.aitech1.ru

PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	62 of 100

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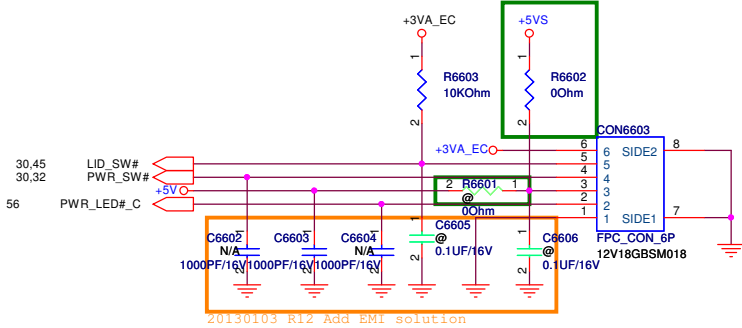
PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	63 of 100

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PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Ser.2		Engineer: <i>Johnson Huang</i>	
Size	Project Name		Rev
A	X750LB		1.1
Date: Thursday, August 01, 2013		Sheet	64 of 100

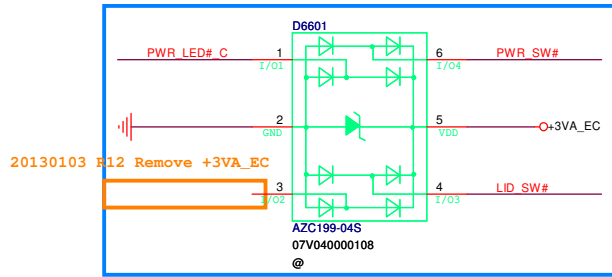
PWR BRD

20130218 R20 Add for S3 Power LED on Power Button off

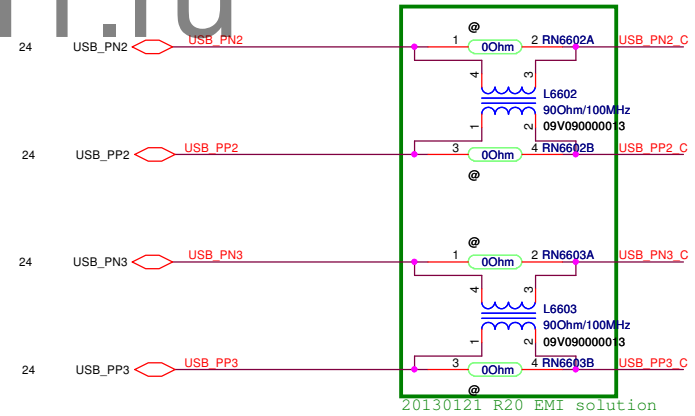
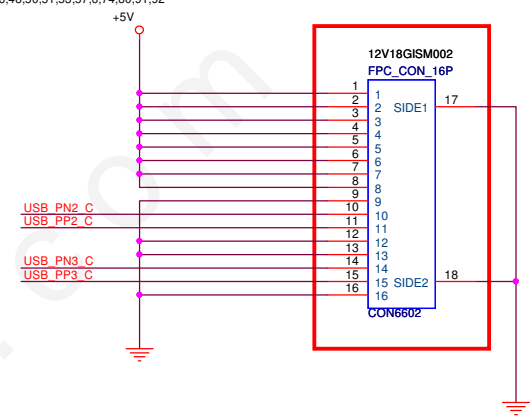


R1.0 0928 Remove debounce(add debounce at PWR BD side)

R1.0 1018 EMI

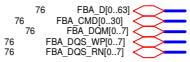


+5V	45,52,57,91
+3VS	16,17,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+5VSUS	22,26,4,51,56,81,83
+3VA_EC	28,30,32,44



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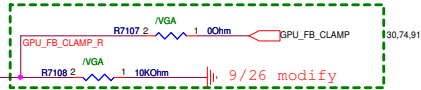
PEGATRON		Title :	
BG1-HW RD Center-HW RD Div.2-HW RD Supp. Hs Sec.2		Engineer: Johnson Huang	
Size	Project Name	Rev	
Custom	Comal	1.1	
Date: Thursday, August 01, 2013		Sheet	67 of 100



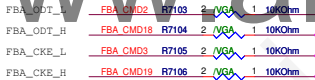
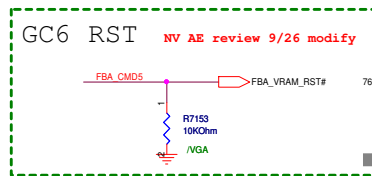
U7001B

FBA_D0	E18	FBA_D0
FBA_D1	F18	FBA_D1
FBA_D2	F16	FBA_D2
FBA_D3	F17	FBA_D3
FBA_D4	D20	FBA_D4
FBA_D5	D21	FBA_D5
FBA_D6	F20	FBA_D6
FBA_D7	E21	FBA_D7
FBA_D8	E15	FBA_D8
FBA_D9	D15	FBA_D9
FBA_D10	F15	FBA_D10
FBA_D11	F13	FBA_D11
FBA_D12	C13	FBA_D12
FBA_D13	B13	FBA_D13
FBA_D14	E13	FBA_D14
FBA_D15	D13	FBA_D15
FBA_D16	B15	FBA_D16
FBA_D17	C16	FBA_D17
FBA_D18	A13	FBA_D18
FBA_D19	A15	FBA_D19
FBA_D20	B18	FBA_D20
FBA_D21	A18	FBA_D21
FBA_D22	A19	FBA_D22
FBA_D23	C19	FBA_D23
FBA_D24	B24	FBA_D24
FBA_D25	C23	FBA_D25
FBA_D26	A25	FBA_D26
FBA_D27	A24	FBA_D27
FBA_D28	A21	FBA_D28
FBA_D29	B21	FBA_D29
FBA_D30	C20	FBA_D30
FBA_D31	C21	FBA_D31
FBA_D32	R22	FBA_D32
FBA_D33	R24	FBA_D33
FBA_D34	T22	FBA_D34
FBA_D35	R23	FBA_D35
FBA_D36	N25	FBA_D36
FBA_D37	N26	FBA_D37
FBA_D38	N23	FBA_D38
FBA_D39	N24	FBA_D39
FBA_D40	V23	FBA_D40
FBA_D41	V22	FBA_D41
FBA_D42	T23	FBA_D42
FBA_D43	U22	FBA_D43
FBA_D44	Y24	FBA_D44
FBA_D45	AA24	FBA_D45
FBA_D46	Y22	FBA_D46
FBA_D47	AA23	FBA_D47
FBA_D48	AD27	FBA_D48
FBA_D49	AB25	FBA_D49
FBA_D50	AD26	FBA_D50
FBA_D51	AC25	FBA_D51
FBA_D52	AA27	FBA_D52
FBA_D53	AA26	FBA_D53
FBA_D54	W26	FBA_D54
FBA_D55	Y25	FBA_D55
FBA_D56	R26	FBA_D56
FBA_D57	T25	FBA_D57
FBA_D58	N27	FBA_D58
FBA_D59	R27	FBA_D59
FBA_D60	V26	FBA_D60
FBA_D61	V27	FBA_D61
FBA_D62	W27	FBA_D62
FBA_D63	W25	FBA_D63

NC	FB_CLAMP
QF119	QF117/GK308



FBA_CMD0	C27	FBA_CMD0
FBA_CMD1	C28	FBA_CMD1
FBA_CMD2	E24	FBA_CMD2
FBA_CMD3	F24	FBA_CMD3
FBA_CMD4	D27	FBA_CMD4
FBA_CMD5	D26	FBA_CMD5
FBA_CMD6	F25	FBA_CMD6
FBA_CMD7	F26	FBA_CMD7
FBA_CMD8	P23	FBA_CMD8
FBA_CMD9	C22	FBA_CMD9
FBA_CMD10	C23	FBA_CMD10
FBA_CMD11	G24	FBA_CMD11
FBA_CMD12	F27	FBA_CMD12
FBA_CMD13	C25	FBA_CMD13
FBA_CMD14	G27	FBA_CMD14
FBA_CMD15	G28	FBA_CMD15
FBA_CMD16	M24	FBA_CMD16
FBA_CMD17	M23	FBA_CMD17
FBA_CMD18	K24	FBA_CMD18
FBA_CMD19	K23	FBA_CMD19
FBA_CMD20	M27	FBA_CMD20
FBA_CMD21	M25	FBA_CMD21
FBA_CMD22	M26	FBA_CMD22
FBA_CMD23	K26	FBA_CMD23
FBA_CMD24	K22	FBA_CMD24
FBA_CMD25	J23	FBA_CMD25
FBA_CMD26	J25	FBA_CMD26
FBA_CMD27	J24	FBA_CMD27
FBA_CMD28	K27	FBA_CMD28
FBA_CMD29	K25	FBA_CMD29
FBA_CMD30	J27	FBA_CMD30
FBA_CMD31	J26	FBA_CMD31



FBA_CLK0	D24	FBA_CLK0	76
FBA_CLK0#	D25	FBA_CLK0#	76
FBA_CLK1	N22	FBA_CLK1	76
FBA_CLK1#	M22	FBA_CLK1#	76

FBA_WCK01	D18
FBA_WCK01#	C18
FBA_WCK23	D17
FBA_WCK23#	D16
FBA_WCK45	T24
FBA_WCK45#	U24
FBA_WCK67	V25

62 mA FB_PLLAVDD_1

FB_PLLAVDD_2

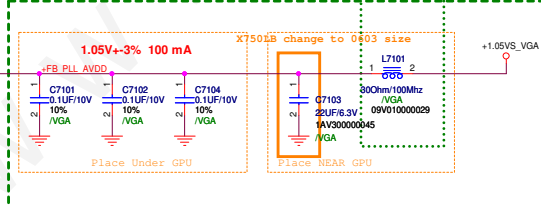
FB_PLLAVDD	FB_DLLAVDD
QF117	QF119/GK308

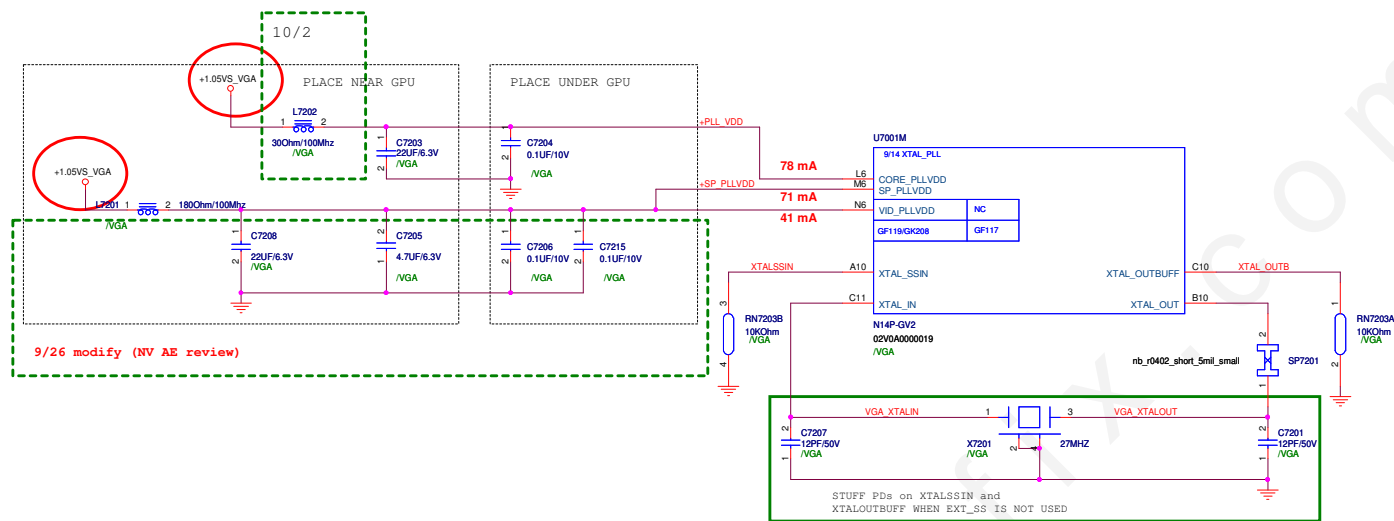
35 mA

R1.0 1108 Remove T7101 for layout



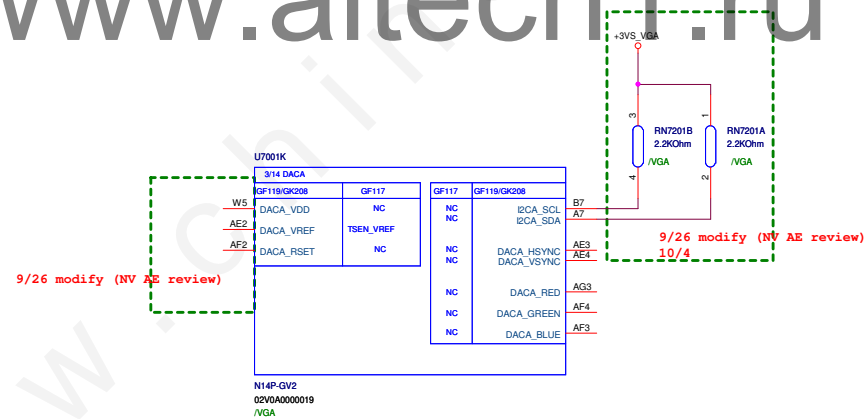
N14P-GV2
02V0A0000019
/VGA



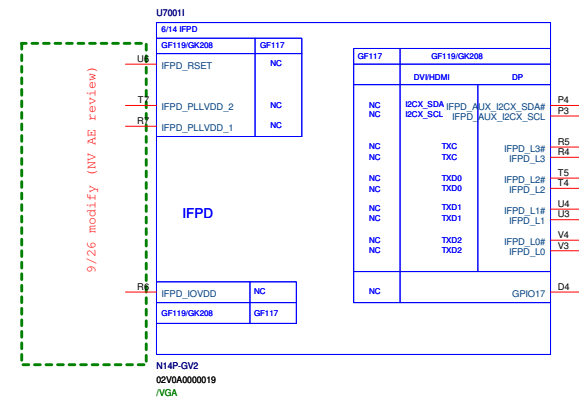
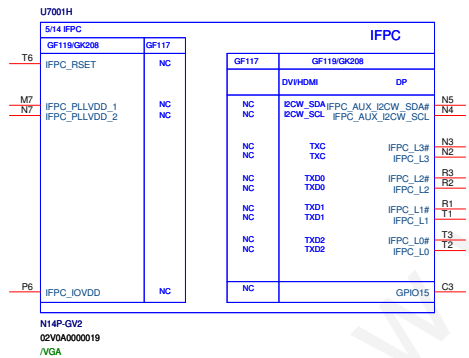
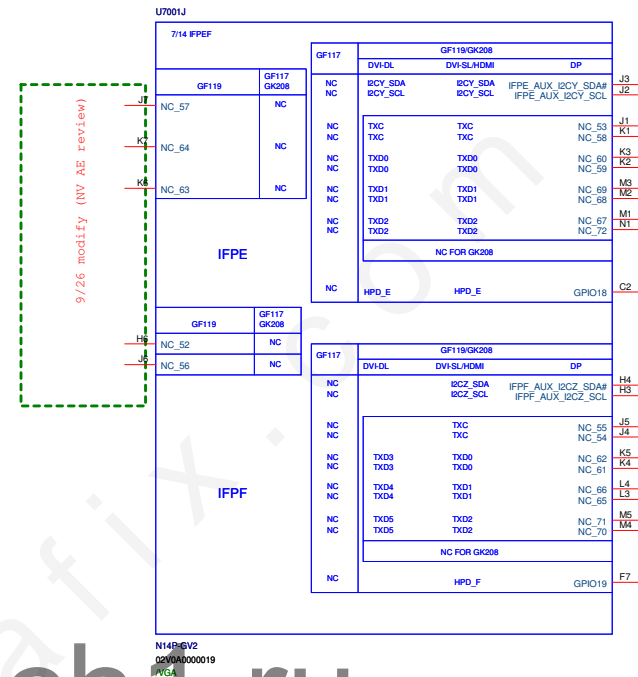
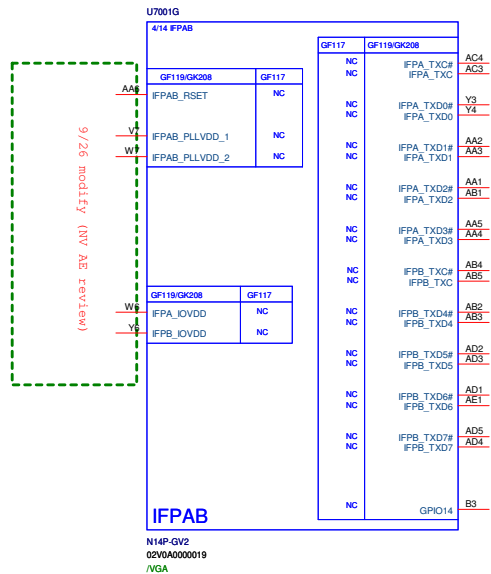


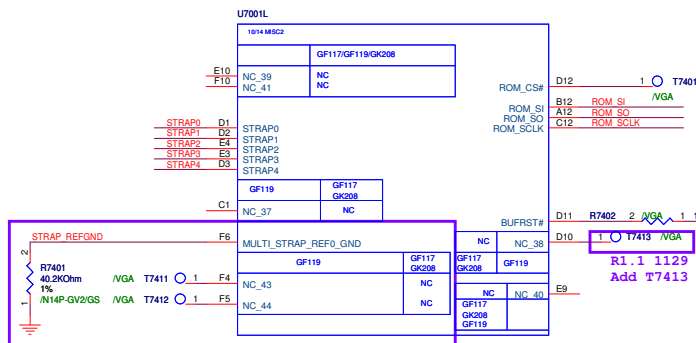
R1.2 1220 TXC recommend to adjust C7201,C7207=12pF

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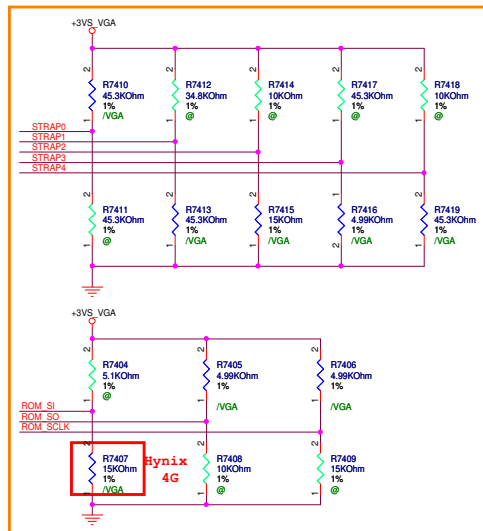


LVDS





R1.1 1128 Modify R7401 connection from pin F5 to F6
Add T7411 & T7412



BINARY STRAP MODE MAPPING for N14M-GL

Pin Name	Mapping	Pull down 10K
ROM_SCLK	SMB_ALT_ADDR	Pull down 10K
ROM_SI	SUB_VENDOR	Pull down 10K
ROM_SO	VGA_DEVICE	Pull down 10K
STRAP0	RAM_CFG[0]	
STRAP1	RAM_CFG[1]	
STRAP2	RAM_CFG[2]	
STRAP3	RAM_CFG[3]	
STRAP4	PCI_MAX_SPEED	Pull down 10K

RAM_CFG[3:0]

Vendor	Part Number	Strap
Micron	MT41JT128M16JT-093G:E	0x1 (0001)
Micron	MT41JT128M16JT-107G:E	0x1 (0001)
Hynix	H5TQ466MFR-11C	0x3 (0011)
Hynix	H5TQ4663APR-11C	0x4 (0100)
Samsung	K4W2G1646E-BC1A	0x5 (0101)
Samsung	K4W2G1646E-BC11	0x5 (0101)
Hynix	H5TQ2G63DPR-NOC	0x6 (0110)
Hynix	H5TQ2G63DPR-11C	0x6 (0110)
Samsung	K4W4G1646B-HC11	0xB (1011)
Micron	MT41K256M16HA-107G:E	0xD (1101)

1: Pull up 10k
0: Pull down 10K

STRAP0 (1,1,1,1 pu 45K)
USER[3:0]
3 2 1 0 PANEL VS/HS
0 0 0 0 XGA
0 0 0 1 XGA
0 0 1 0 SXGA
0 0 1 1 SXGA+
0 1 0 0 DPGA
0 1 1 1 SHD N/A

STRAP1 (0,0,0,0 PD 5K)
3GIO_PADCFG[3:0]
3 2 1 0
0 0 0 0 Gen1 support
0 1 1 0 Gen1/Gen2 only
others RESERVED

STRAP2 (0,0,1,0 PD 15K)
for GV2 QS
LOGICAL BIT
0 PCI_DEVID[0]
1 PCI_DEVID[1]
2 PCI_DEVID[2]
3 PCI_DEVID[3]

STRAP3 (0,0,0,0 PD 5K)
LOGICAL BIT
0 SOR0_EXPOSED
1 SOR1_EXPOSED
2 SOR2_EXPOSED
3 SOR3_EXPOSED

ROM_SO (1,0,0,0 PU 5K)
3GIO_PADCFG[3:0]
LOGICAL BIT
3 FB[1]
2 FB[0]
1 SMB_ALT_ADDR
0 VGA_DEVICE

ROM_SCLK (1,0,0,0 PU 5K)
for GV2 QS
LOGICAL BIT
3 PCI_DEVID[4]
2 SUB_VENDOR
1 PCI_DEVID[5]
0 PEX_PLL_EN_TERM

STRAP4 (0,0,0,1 PD 10K)
LOGICAL BIT
0 DP_PLL_VDD33V
1 PCIE_MAX_SPEED
2 PCIE_SPEED_CHANGE_GEN3
3 RESERVED

GB4-128

5K	10K	15K	20K	25K	30K	35K	45K
PU	1000	PD	0000				

PCI_DEVID[3..0]
N14P-GV2 --> 0X1292 ~ 0 0 1 0 --> pull down 15K

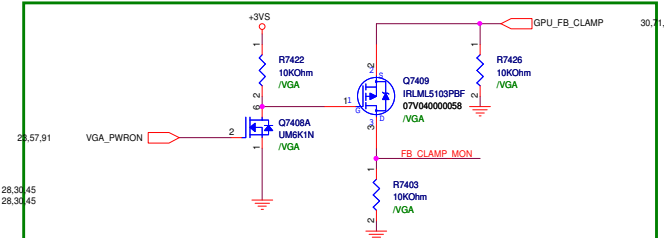
ROM_SI RAMCONFIG (0,1,0,1 PD 30K)
Micron 256Mx8
RAM_CFG[3:0]

Vendor	Part Number	Strap
Micron	MT41K256M8DA-125:M	0x5 (0101)
Micron	MT41K512M8RH-125:E	0x1 (0001)
Hynix	H5TC2G83EFR-PBA	0x6 (0110)
Hynix	H5TC4G83AFR-PBA	0x2 (0010)

R1.2 0107 NV change strapping of Hynix 4G

MULTI-LEVEL MODE STRAPPING for N14P-GV2/GS

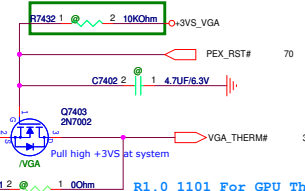
R1.2 0102 Add R7403, R7422, R7426, Q7409 for NV GC6 function



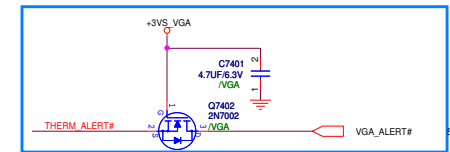
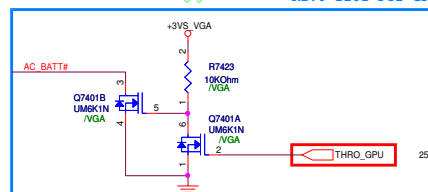
R1.2 0102 Modify R7428 for GC6 function NV Suggestion

R1.2 0102 PU 10K ohm move to EC side

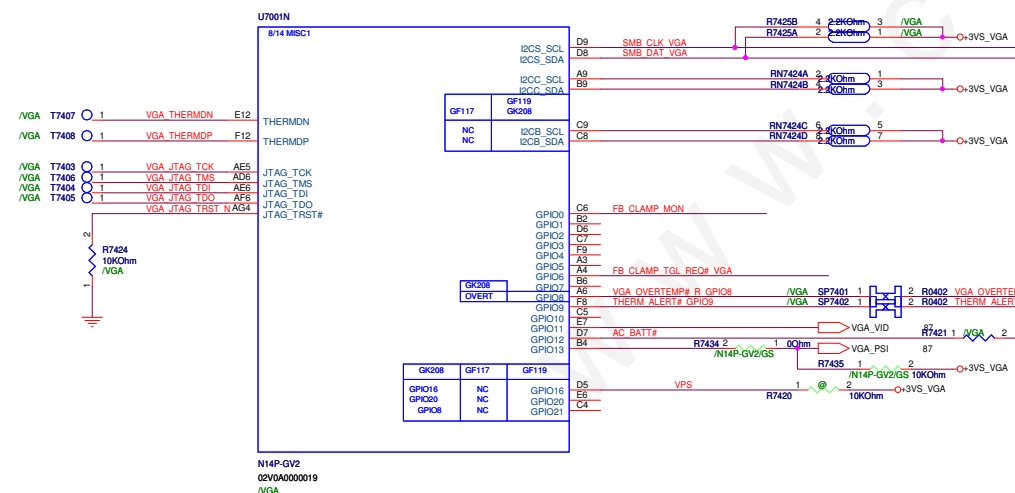
R1.2 1228 Set R7432 un-mount



R1.0 1101 For GPU Throttle

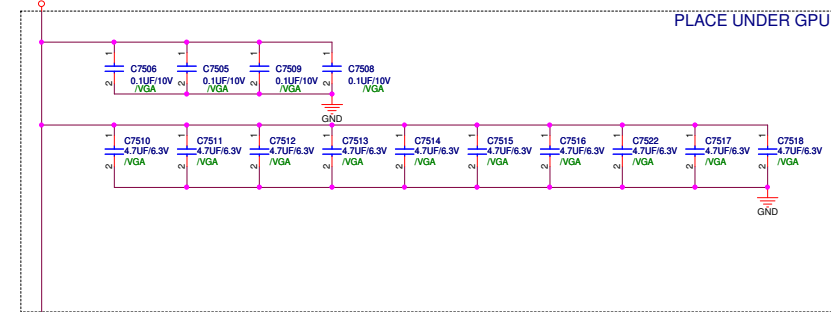
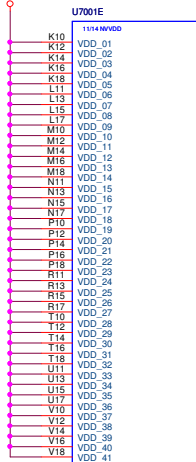


R1.0 1031 ADD VGA_ALERT# (Thermal sensor to GPU)

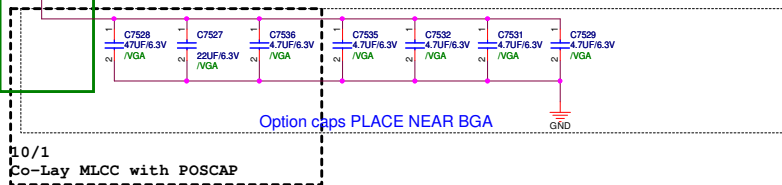


+VGA_VCORE

+VGA_VCORE



R1.2 1227 Remove CE7501(0) for layout

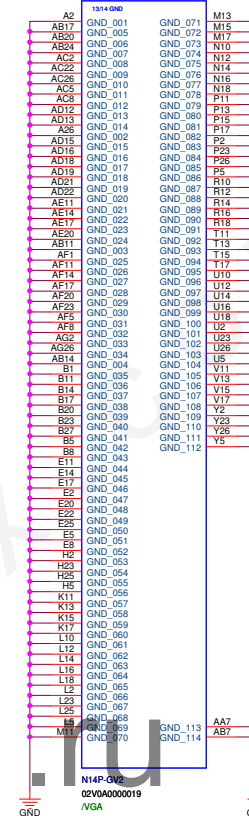


10/1
Co-Lay MLCC with POSCAP

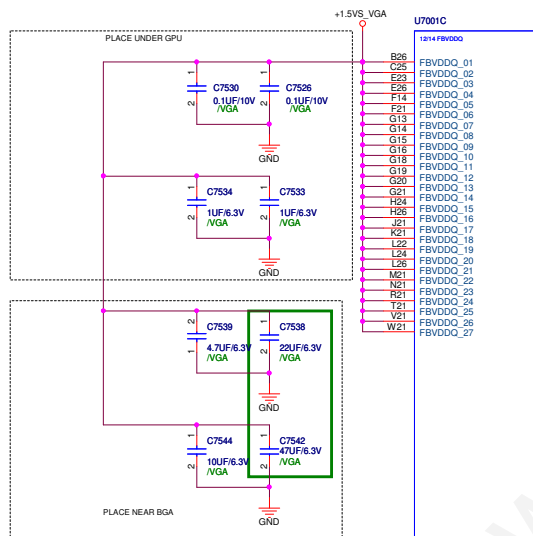
NV Design Guide
For GB4-128
4.7u x 10/15 (0603)
0.1u x 4/8
47u x 1/1
22u x 1/7
4.7u x 5/6 (0805)
330u x 0/1

NV Design Guide
For GB2-64
4.7u x 10/10 (0603)
0.1u x 4/4
47u x 1/1
22u x 1/1
4.7u x 5/5 (0805)
330u x 0/1

U7001F

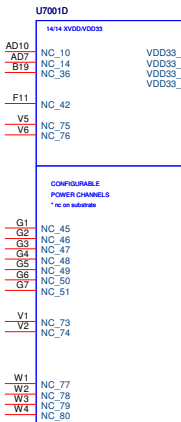
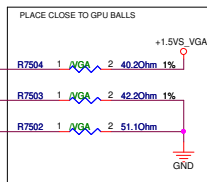


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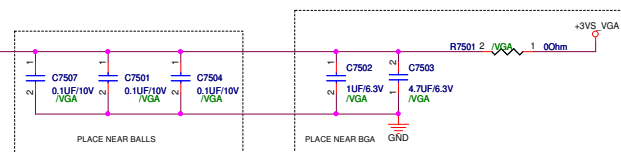


R1.2 1220
C7538 change to 22uF
C7542 change to 47uF

N14P-GV2
02V0A0000019
/VGA

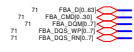


N14P-GV2
02V0A0000019
/VGA

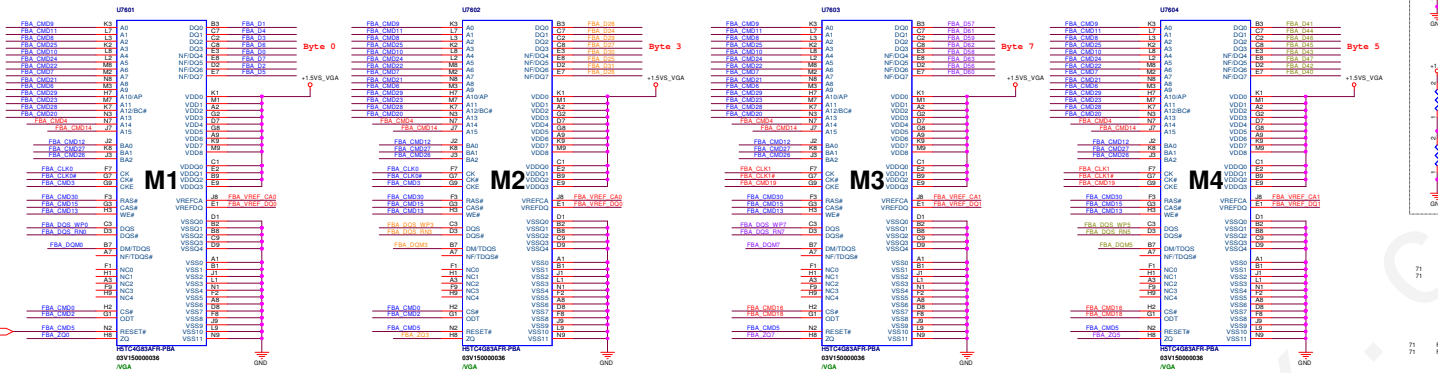


VRAM CH A

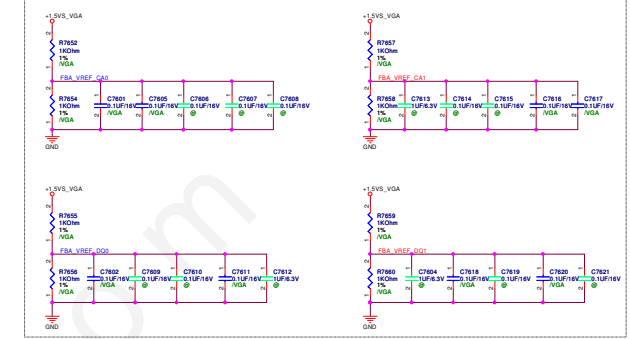
Mode D Command Mapping



TOP SIDE --- M1, M2, M3, M4



place near VRAM



NVIDIA Spec. 建議值為160 ohm

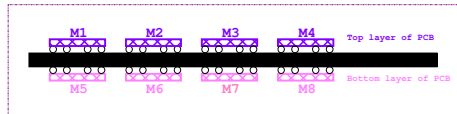
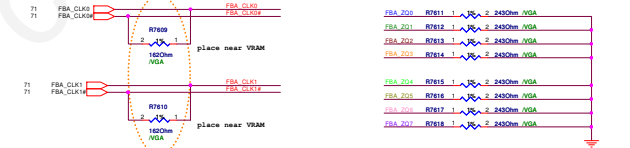
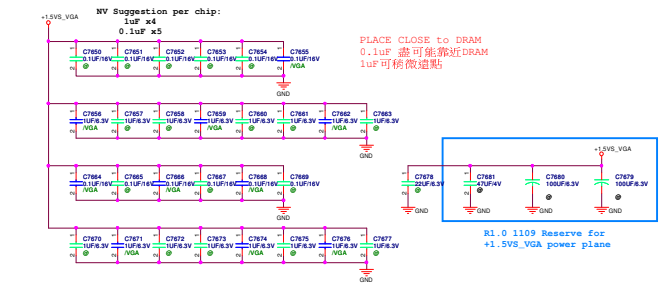
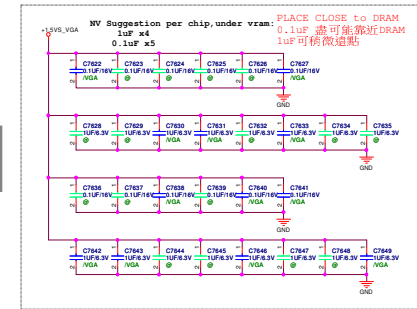
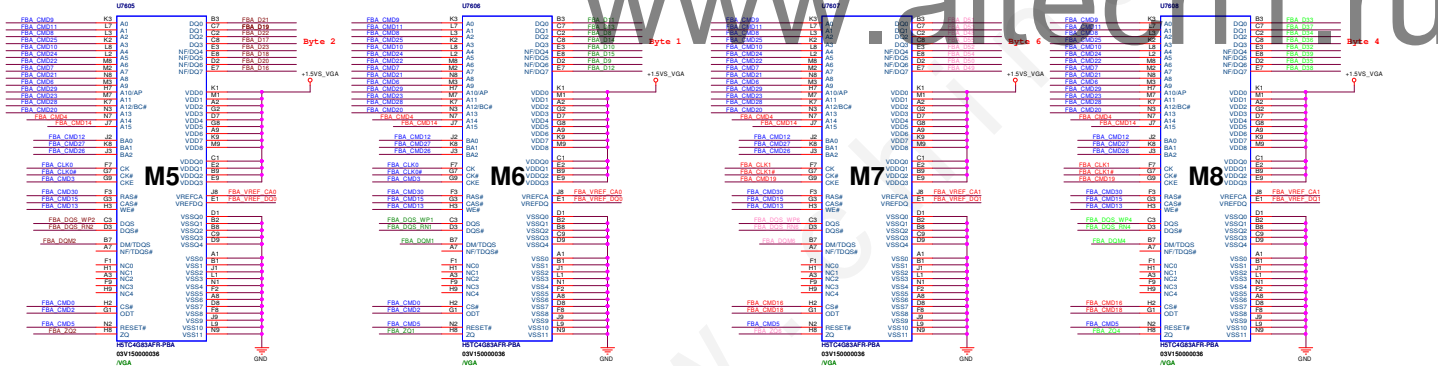


Table 29. Combined/Separate Memory FBVDD/Q Decoupling DDR3 x16 with DRAM on One Side

Capacitor Type	Population* for Combined FBVDD/FBVDDQ	Population* for Separate FBVDDQ	Location
0.1 uF X7R 0402	2	4	2
1.0 uF X7R 0603	4	3	1

*For memory chip.

BOTTOM SIDE --- M5, M6, M7, M8



VRAM CH C

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R1.0
delete Ventura.

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PEGATRON		Title :VGA_VENTURA_INA219	
BG1-HW RD Center-HW RD Div.2-HW RD Div.2-HW RD Sec.2		Engineer :Johnson Huang	
Size	Project Name	X750LB	Rev
B	P/N	<OrgAddr2>	1.1
Date: Thursday, August 01, 2013		Sheet	78 of 100

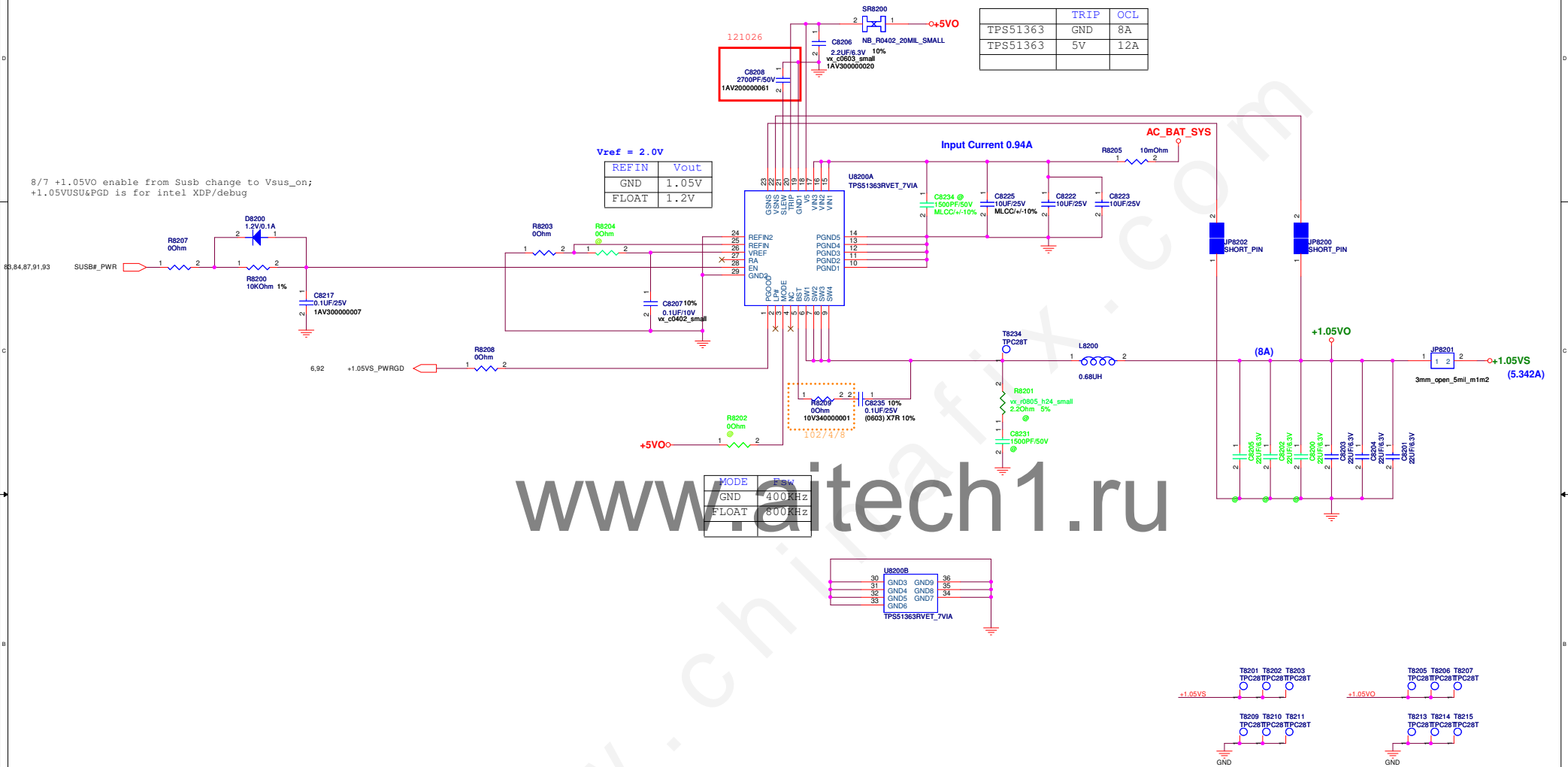
R1.0

delete GB3-128 additional schematic.

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PEGATRON		Title : ADDITIOAL	
BG1-HW RD Center-HW RD Div.2-HW RD Dept.2 RD Sec.2		Engineer: Johnson Huang	
Size A	Project Name P/N	X750LB <OrgAddr2>	Rev 1.1
Date: Thursday, August 01, 2013		Sheet	79 of 100

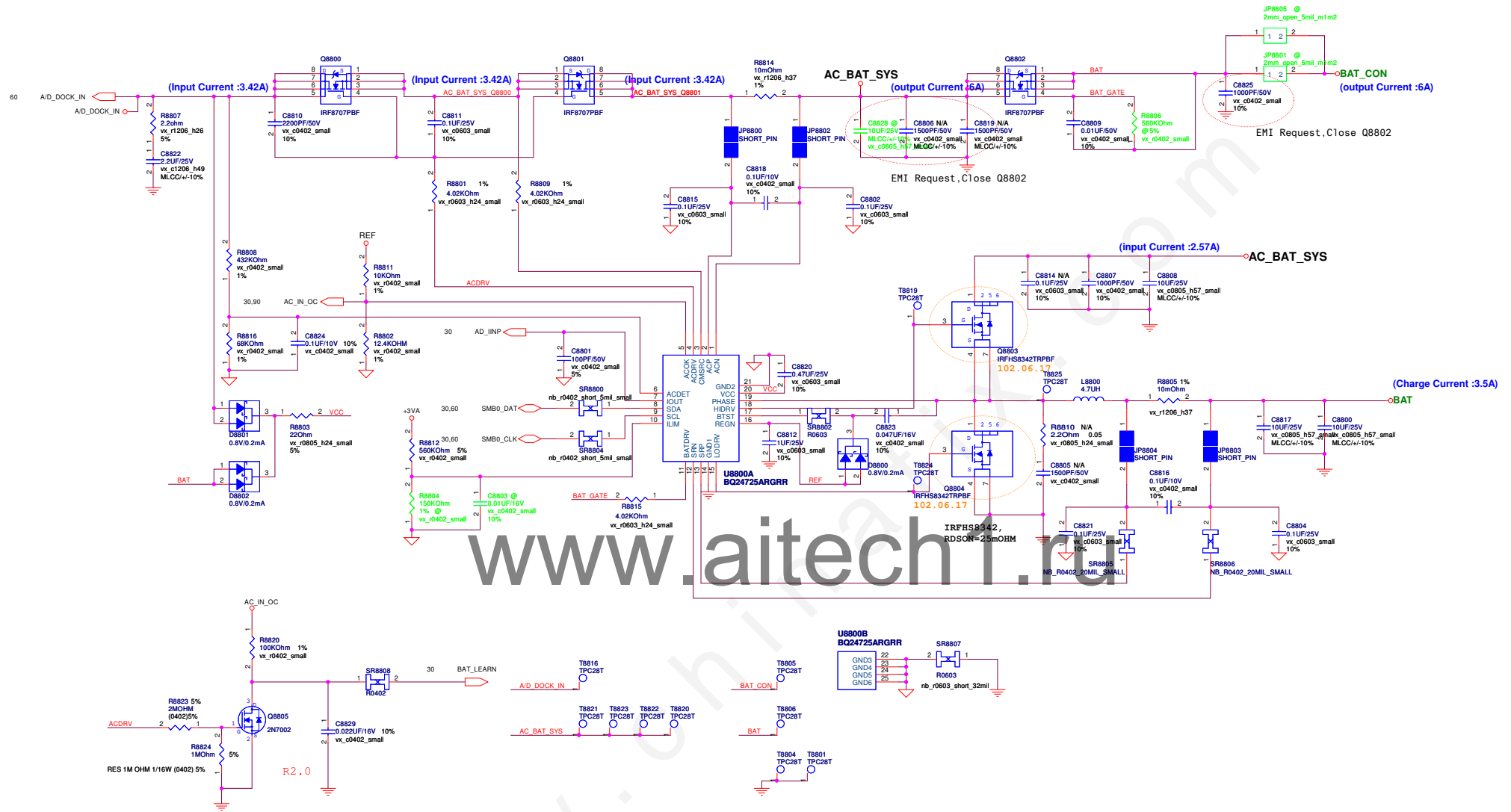
+1.05VS POWER SUPPLY



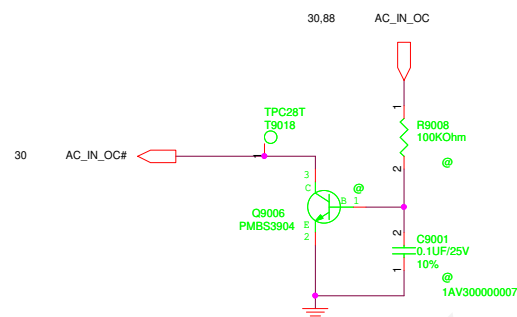
www.aitech1.ru

<Variant Name>		
PEGATRON Title : POWER_1.8VS		
Engineer: Benson Lin		
Size	Project Name	Rev
Custom	X750LB/LA	1.0
Date: Thursday, August 01, 2013 Sheet 95 of 94		

BATTERY CHARGER



ADAPTER IN DETECT

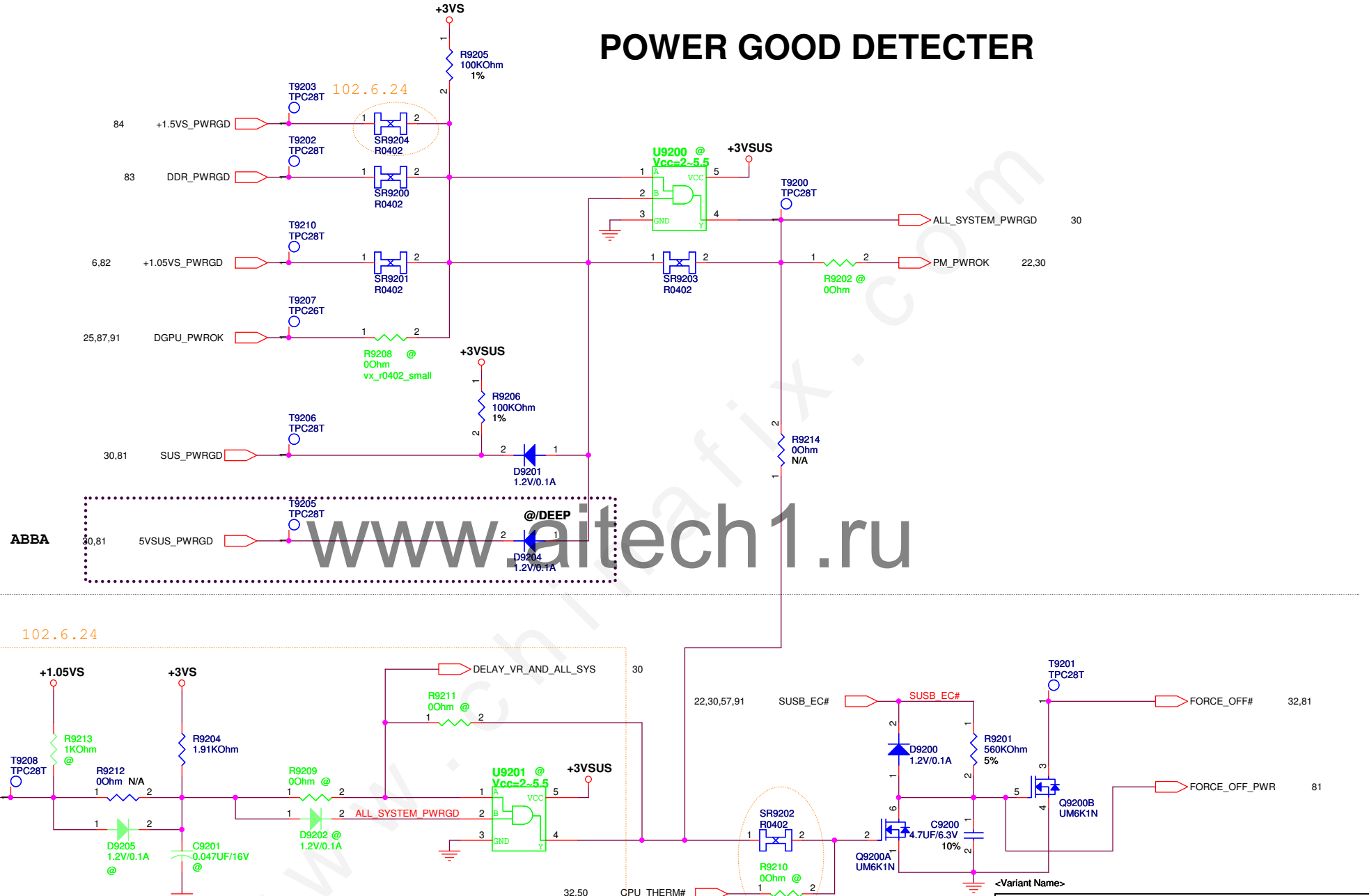


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<Variant Name>

PEGATRON		Title : POWER_DETECT	
		Engineer: Benson Lin	
Size Custom	Project Name X750LB/LA	Rev 1.0	
Date: Thursday, August 01, 2013		Sheet 90 of 99	

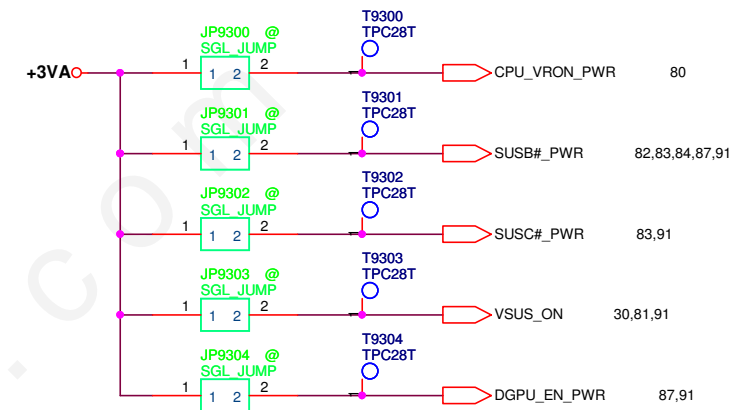
POWER GOOD DETECTOR



PEGATRON				Title : POWER_PROTECT	
Engineer: Benson Lin					
Size	Project Name				Rev
Custom	X750LB/LA				1.0
Date: Thursday, August 01, 2013			Sheet 92 of 94		

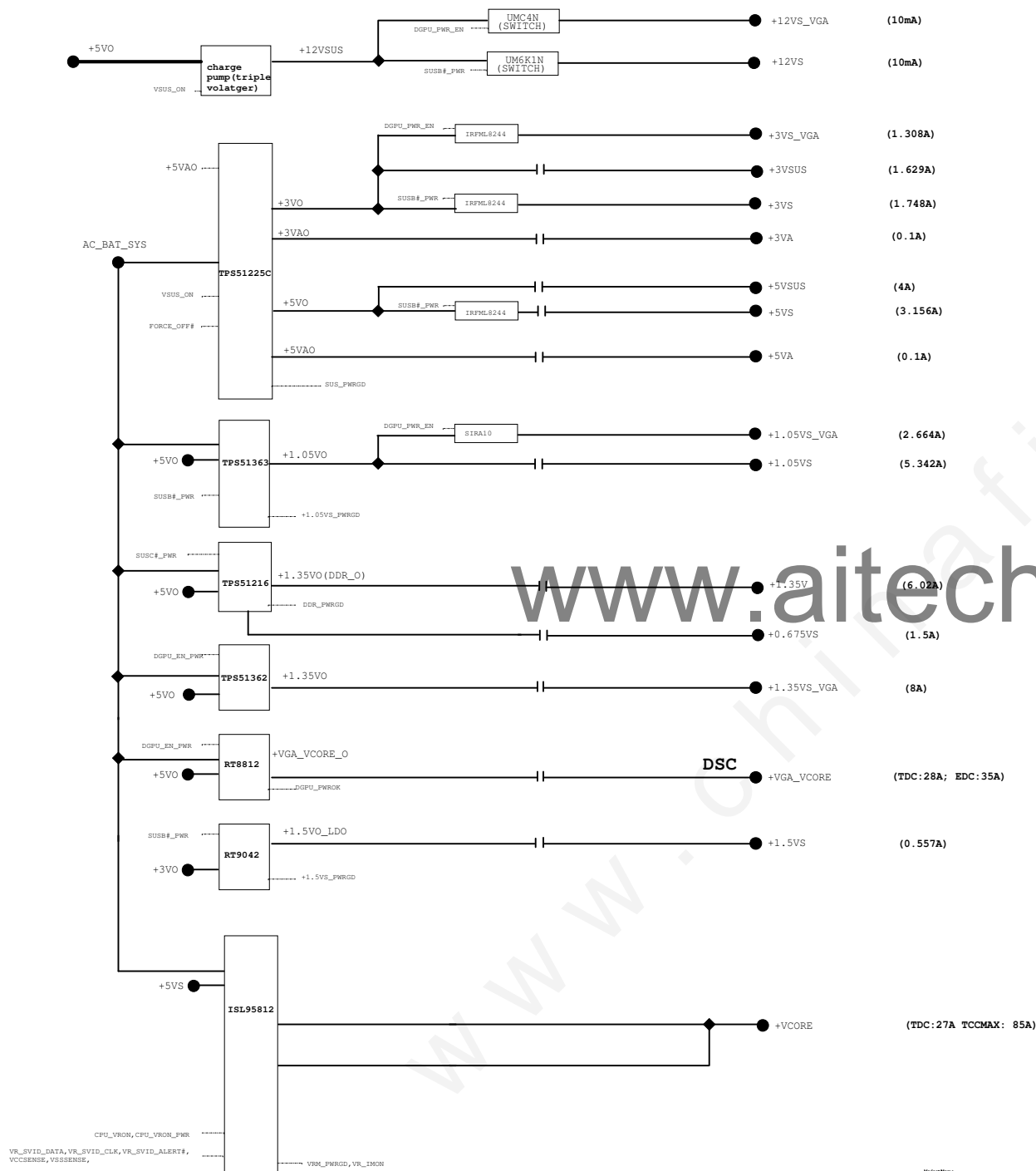
AC_BAT_SYS	AC_BAT_SYS	45,80,81,82,83,84,87,88
BAT_CON	BAT_CON	60,88
+5VA	+5VA	81,91
+3VA	+3VA	20,26,30,57,81,88,91
+5VO	+5VO	81,82,84,91
+3VO	+3VO	81,91
+1.05VO	+1.05VO	82,91
+12VSUS	+12VSUS	22,26,51,81,91
+5VSUS	+5VSUS	22,26,4,51,56,81,83
+3VSUS	+3VSUS	22,26,28,30,33,34,53,81,92
+12V	+12V	91
+3V	+3V	22,45,57,91
+12VS	+12VS	28,31,46,5,57,91
+5VS	+5VS	20,30,36,46,48,50,51,56,57,66,80,87,91
+3VS	+3VS	16,17,20,21,22,23,25,26,28,30,31,32,33,36,37,4,40,44,45,46,48,50,51,53,57,6,74,80,91,92
+1.5VS	+1.5VS	26,53,57,84
+1.05VS	+1.05VS	25,26,32,46,57,6,80,82,92
+VCORE	+VCORE	6,80

FOR POWER TEST



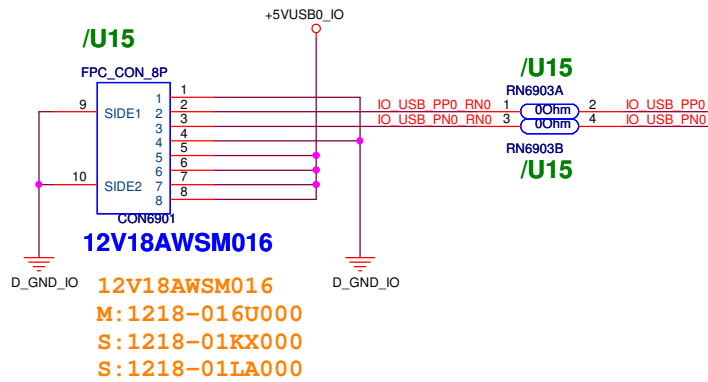
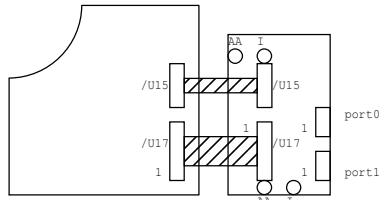
<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Benson Lin	
Size	Project Name		Rev
Custom		X750LB/LA	1.0
Date: Thursday, August 01, 2013		Sheet	93 of 94

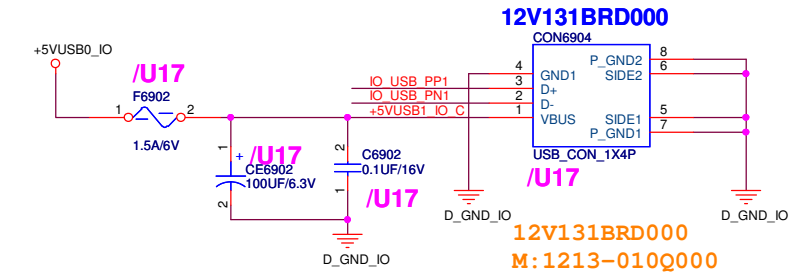
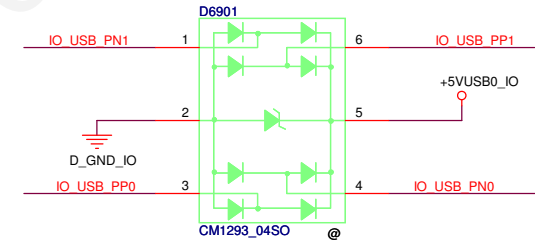
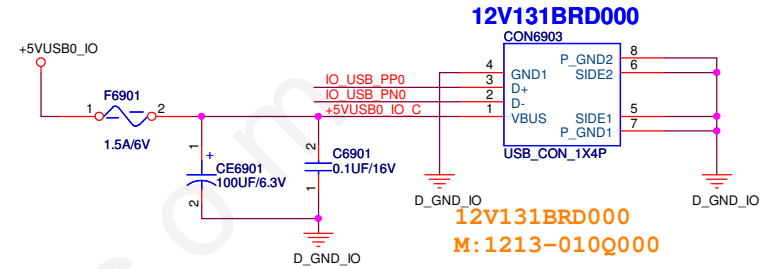
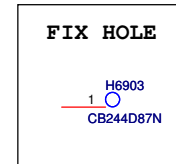
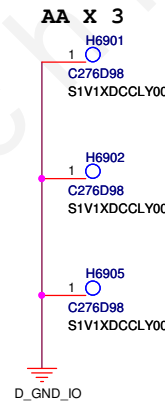
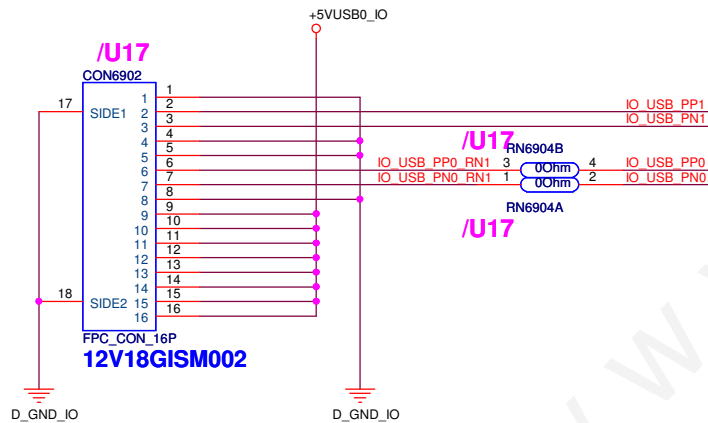


USB 2.0

USB 2.0 for 17"

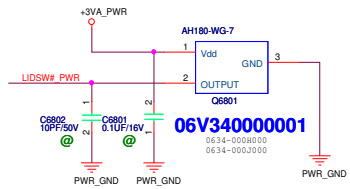


17" pin 5 對應 15" pin1

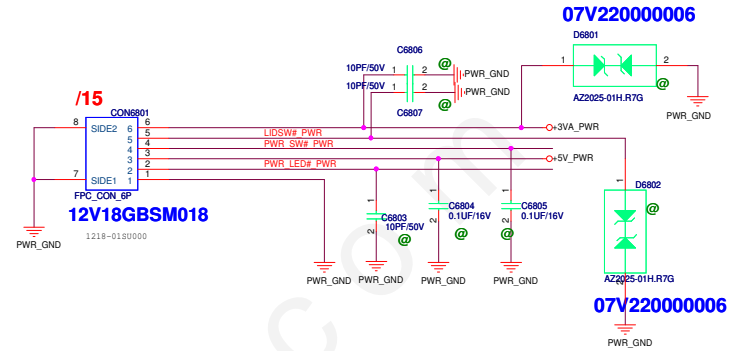
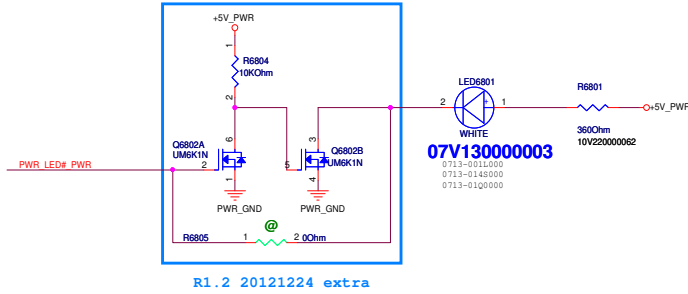


PEGATRON Title :IO		
BG1/RDCenter Engineer: Osmand Fang		
Size B	Project Name X750DP	Rev 1.0
Date: Thursday, August 01, 2013	Sheet 95 of 96	

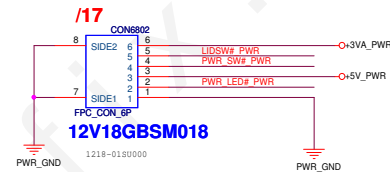
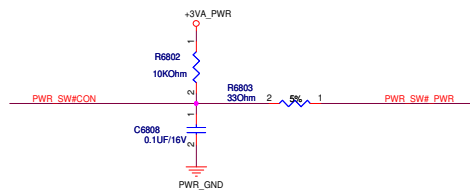
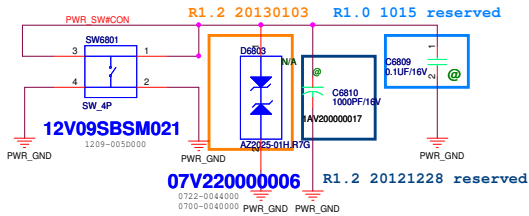
Hall Sensor



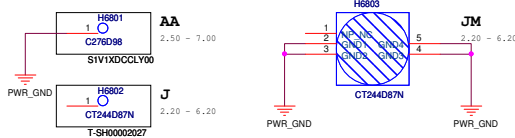
Power LED



Power Button



Ground Hole & Pad



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20130624
R2059, R2052, R2055, R3604 changed to SP2001, SP2002, SP2003, SP3601
Reserve F4501
Add C5113, C5111, C5127, C5128, C5123, C5124
Change H6514 for ME request
Delete H6521

20130625
R2057 change to SP2004
C7529, C7531, C7532, C7535, C7536 changed to 0805
C7679, C7680, C7681 changed to 3216 PosCap
Delete R2038-R2043
PCIE_RCOMP, PCIE_IREF PU from +1.05 to +1.05VS_AUSB3PLL
SATA_IREF PU from +1.05 to +1.05VS_ASATA3PLL
Mount R0411, R2026, R2223, U2201
Unmount R2202, U2002
Change R2123, R2124 to 0ohm
Add R1818, R1819, R1821, R1822, R1815, R1816, C1804, C1807, C1805

20130626
Add R4617-R4619
Change U4601 to VX PN
Delete T2539
U4601.3,4 connect from SMBus to I2C

20130627
Add R4620, R4621
Change SP5202, SP5203 to R5212, R5213
Reserve R5222, R5223
Change R2235 option to /nonINTEL_DS3
Reserve R3036, R3037, R0401, R0403, R0404, R2102
Change D6601, D4504

20130628
R2007 connect from +1.05VS to +1.05VS_ASATA3PLL
Reserve RN4601, RN4602, RN4603, Q4603, Q4602, U4602, U4603

20130630
Reallocate R4620, R4621 on the place between Q4602 and CON4602
Change RN4601 and RN4602 to 4.7kohm

20130701
Delete H6562

20130702
Change C7103 to 0603 size

20130703
Reserve R2238

20130709
Unmount C2611; Change R2615 to 0ohm
Reserve R3038, R3039

20130717
Reserve C3410, C3411
Change R2401 to 3.01Kohm
R2640, R2637 connect to DCP8US

20130719
Change DS3_AC from GPG2 to GPI7

20130720
Delete SP3005

20130722
Change R3050 option to 8
Mount R0502, R5111, R5112, R5113

20130724
Change all capacitors on GPU site to 0.1uF for PCIE GEN2

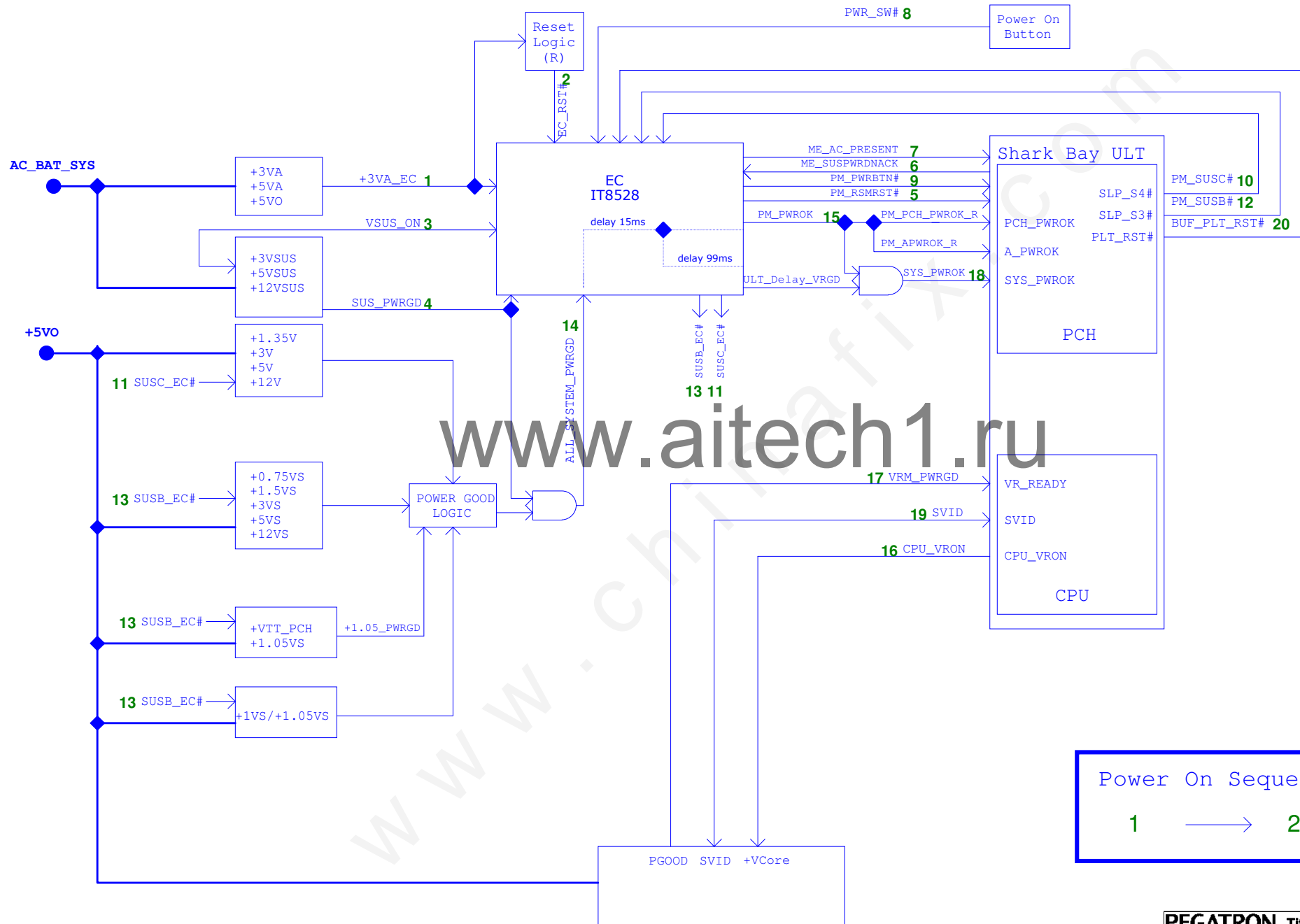
20130725
Unmount R4613, R4614

20130730
Add R2618, R2619

20130731
Reassign PCIE CLKREQ and add R2125, R2132, R2133

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Power On Sequence Diagram G3-S0 R0.3 (non-iAMT,non-Deep Sx)



Power On Sequence

1 → 20

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)

